DESIGN OF AN AUTONOMOUS UNDERWATER VEHICLE (AUV) CHARGING SYSTEM FOR UNDERWAY, UNDERWATER RECHARGING

by

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14. ABSTRACT

Modern robotics have enabled the rapid proliferation of Autonomous Underwater Vehicles (AUVs) throughout the marine environment. As autonomy algorithms increase in robustness, complexity, and reliability, so too does the ability of AUVs to perform an even-increasing array of complex missions. Maritime tasks that once required a fleet of ships, months to complete, and numerous mariners are now being performed by AUVs with little to no logistical support elements. Despite the many AUV technology advances that have been made, power remains a limiting factor. Most AUVs use onboard stored electric energy and electric drive to perform their various missions. The current method for deploying this type of AUV requires charging it above water, shipping it to a mission site, and then deploying it overboard with the use of cranes. The AUV is then recovered once the mission is complete or ? more likely ? when its power source is depleted. The deployment and recovery phases are time-intensive, limited by weather conditions and sea state, and often hazardous to both crew and AUV. While deployment and recovery will remain critical, high-risk evolutions, there exists a need to find a safer and faster recharging method that does not require recovery of the vehicle. This thesis addresses a fraction of the underwater AUV power transfer and rapid charging challenge through the development of the power electronics required to reliably charge a single battery pack. Power is supplied inductively to a receiver coil in the AUV. This power is then transferred to a down converter with a current-sensing feedback controller to provide a regulated current under the varying load voltage of the battery pack. The system is capable of providing up to 500W of instantaneous power to a single pack. It is electrically isolated from the power source through the use of an input transformer and is compact enough to be integrated into an AUV for future testing.

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Contents

List of Figures

List of Tables

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Aleksandar Misic and Michael Defilippo were my projects colleagues and helped tremendously. Aleks is characterizing and designing the power cell and battery management system for the final system. Michael is working on developing a new inductive charge transfer coil for power transfer over distances of 10+ cm in saltwater.

Finally, I would like to thank the exceptional engineers working for NAVSEA who provided assistance and insight along the way. In particular, I owe a great deal of thank to Peter Hadro from NUWC Newport and Joe Curran from NSWC Carderock for their support and insight over the course of this project.

1. Introduction

The design work presented herein was conducted in collaboration with MIT SEA GRANT College Program through funding provided by the Office of Naval Research (ONR). This work is intended to be used to fulfill the research objectives stated in the Research Project Proposal, "Wireless Recharging of Autonomous Unmanned Vehicles (AUVs) while Underway" [1].

Key research tasks are outlined in [1]. The task directly associated with this work is Task 2: the design of an AUV wireless-charging device and connection system. The design focus was isolated to the charging system. Power electronics are required for this application to provide rapid, "smart" charging of the battery cell without damage. Charging requires a well-conditioned, well-regulated DC charging current. For this thesis, a buck converter with current regulation was designed, built, and demonstrated to supply a 10A DC current to a battery cell for rapid charging of an underway AUV. The performance of the design is evaluated in detail. Key performance criteria include system efficiency, heat management, and transient response. Because the system is intended to be built into a volume-restricted AUV, size and weight were also important designed parameters driving the selection of a 600kHz switching frequency.

Additional research and work is in progress to develop the power storage cell system and desired wireless power transfer capable. MIT SEA GRANT envisions being able to rapidly recharge AUVs in a seaway without the need to recover the AUV or man the surface vessel responsible for providing charging power. This capability is of particular interest for both commercial and military applications.

A successful demonstration of rapid underway AUV recharging has the potential to greatly decrease AUV deployment and maintenance costs as well as increase mission availability. The ultimate objective of this research is to increase AUV time on station and decrease AUV downtime associated with customarily long deployment/capture, data download, and recharge cycles. A given AUV outfitted with the charging system envisioned will perform its design mission for a much larger portion of its lifecycle as compared to AUVs currently in use.

1.1. Background

While the charging system being developed could be fielded more generally in any remotely-piloted vehicle, the focus of this thesis is on AUVs and AUV applications. AUVs have been around for approximately 60 years. Since inception, they have evolved from little more than toys to fully autonomous platforms often outfitted with some of the most technologically advanced and sophisticated sensors. As their complexity has increased, so has their application. Nowadays, AUVs are employed for an impressive array of commercial and military tasks. The list of tasks AUVs are capable of performing continues to grow as new needs arise and both onboard power and artificial intelligence permit. The focus here will be on the most common industries and their particular AUV applications.

1.1.1. AUV Tasks in the Marine Environment

The oil and gas industry remains perhaps the largest employer of AUVs. The industry uses AUVs to survey the ocean floor to help find new well sites. They cost less, provide better data, and are capable of covering larger areas than surface vessels conducting the same work. Over time, oil and gas industries have expanded their use of AUVs as strictly surveying platforms to perform a variety of other

specialized tasks. These tasks include: geohazard/clearance surveys; rig site surveys; acoustic inspection of pipelines and sub-sea installations; pipeline route surveys; and construction site surveys [2].

The telecommunication and subsea mining industries also use AUVs, though to a lesser extent than oil and gas [2]. The telecommunication industry performs surveying and cable laying with AUVs while the mining industry is mostly conducting more standard AUV surveying missions. AUVs are also used quite heavily by researchers and scientist, with oceanographic surveying being the principle mission. A variety of onboard sensors, however, also support the work of marine biologist and researchers. Cameras, turbidity cells and temperature sensors, as well as acoustic gear, allow marine populations to be studied and an evaluation of the overall health of a given marine environment to be made. Academia is constantly finding new uses for AUVs, as evident by much of the work conducted at MIT SEA GRANT.

More recently, an AUV has been used to scour the ocean floor for missing Malaysian Airlines flight MH370 [3]. MH370 disappeared from air radar on 08 March 2014 and is suspected to have been lost at sea. A Bluefin Robotics Bluefin-21 has been used extensively in the search for wreckage, though to date nothing has been found. This task would be much more difficult and timely with a manned system.

The tasks an AUV can perform has largely been limited by available onboard energy and artificial intelligence. Energy provides endurance while artificial intelligence expands the complexity of tasks that be performed safely and reliably by the AUV. As both increase, the spectrum of AUV applications widens. No doubt industry will continue to find interesting tasks for future AUVs to perform.

The United States Navy is also very interested in developing an organic “fleet” of AUVs to perform a variety of warfare missions. These tasks/missions are most clearly defined in “The Navy Unmanned Undersea Vehicle (UUV) Master Plan” published in 2004 [4]. In order of priority, the tasks the Navy envisions AUVs being capable of performing are [4]:

1. Intelligence, Surveillance, and Reconnaissance (ISR)
2. Mine Countermeasures (MCM)
3. Anti-Submarine Warfare (ASW)
4. Inspection / Identification
5. Oceanography
6. Communication / Navigation Network Node
7. Payload Delivery
8. Information Operations
9. Time Critical Strike

Certainly, no single AUV will be capable of performing all nine tasks. However, a fleet of several AUVs with varied payloads might be able to accomplish all these tasks. Currently, the Navy has demonstrated limited capability and success with AUVs performing a variety of ISR, MCM, and Oceanography missions.

As previously stated, one limitation to developing AUVs capable of performing all of these tasks reliably is the availability of onboard power. The development of a rapid charging method with no need to

remove the AUV from the marine environment would greatly advance the Navy's efforts to perform all the tasks it envisions AUVs performing in the future.

1.1.2. General Arrangement of a Notional AUV

Some very interesting AUV architecture research was conducted by Daniel French in 2010 at the Naval Postgraduate Institute in Monterey, CA. French's work focused on evaluating available AUV form factors and capabilities to determine an optimal architecture for naval applications specifically [4], but his results can be applied to the general case. After surveying multiple AUVs, French evaluated seven of the most widely used platforms, compared them, and then made recommendations with respect to architecture for future AUV development.

Probably the most important recommendations made by French was form-factor. In keeping with the most popular modern AUV designs, French recommended all naval AUVs have a torpedo form factor with faired nose and afterbody [5]. He further recommended the main body be of cylindrical construction with a diameter no greater than 21". 21" is a United States Navy specific criteria designed to permit AUVs deployable from a MK67 torpedo tube. This diameter is also in keeping with the majority of commercially available AUVs and is a reasonable limit to consider. Length is also a factor that needs to be considered. French recommend a length remain less than 5m in keeping with the current length of US Navy MK-48 ADCAP torpedo.

If a torpedo-shaped AUV is assumed, then the general arrangement of such an AUV is illustrated in Figure 1. The forward end of the vessel is dominated by structure and electronic equipment. The electronic equipment includes both processing components such as the main computer and all sensors. Navigation equipment is contained in this portion of the AUV. This section can also be referred to as the payload.

Aft of the payload is the power source. The power source typically some sort of battery pack, the chemistry of which varieties from platform to platform. Modern battery packs are often of Li-Ion polymer construction due to the high power density available in these chemistries.

The aft section of the AUV is reserved for propulsion and control surfaces. Propulsion is typically provided through a single shaft, single propeller design. Ducting is also often used to increase propulsive efficiency.

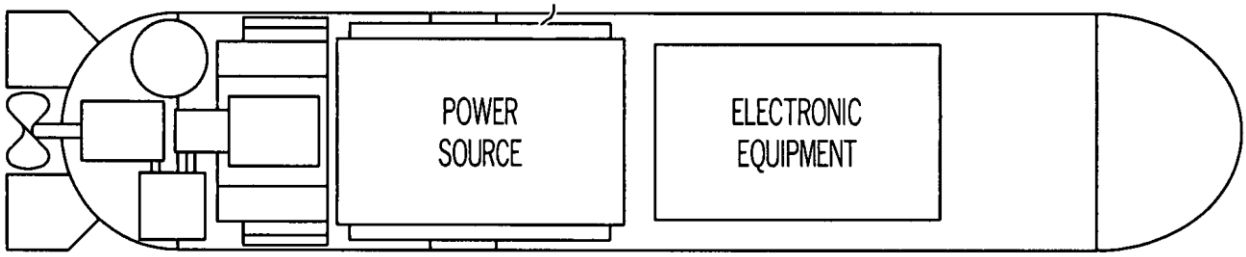

Figure 1: General Arrangement of a Notional Torpedo-Shaped AUV

With Figure 1 in mind, a complete list of French's recommendations can be provided. He recommended aft control surfaces with forward control surfaces optional, a single ducted propeller, a depth rating of 600m, a 24-hour endurance with greater than 5kWh of installed power, an overall length of

approximately 4m, and dry weight less than 300kg. These recommendations require some explanation, which is provided in French's report [5]. They are presented here merely to provide the reader with a sense of the size and construction of the typical AUV for commercial and military applications.

1.1.3. Normal Method of Deployment and Charging

Few AUVs are capable of being handled by a single person. Usually a team of people are required. In fact, most AUVs require a crane for all handling evolutions, to include deployment and recovery. An evolution is a series of coordinate events that must take place to accomplish a specific task, such as system deployment from a surface vessel.

One such handling crane used by the Kongsberg REMUS 600 is shown in Figure 2. The REMUS 600 Launch and Recovery System (LARS) is rather easy to use once installed onboard an acceptable vessel. It needs to be installed though, which is costly in terms of both time and money. Other similarly sized AUVs like the Bluefin-21 require similar deployment and recovery mechanisms. The bottom line is support equipment is required; the AUV cannot be handled without it.

Because support equipment is required, deployment of the AUV is very costly. It requires the purchase or chartering of an acceptable surface platform, the installation of support equipment, and finally on station time as the AUV must be recovered either upon completion of its mission or when its power source is depleted. Launching and recovery is also costly in terms of system failures. The AUV is most vulnerable to damage when it is suspended from its retaining cable in the process of being deployed or recovered. The cable could snap, wave action on the vessel could cause the AUV to impact the deck or support structure, etc. The potential for serious impact and damage is greatest during these evolution.

Figure 2: REMUS 600 Launch & Recovery System (LARS) [6]

Charging is typically accomplished by removing the AUV from the water and plugging its power cell into an appropriate power supply. The charging process is slow, limited by the safe charging rate of the battery pack or the complete disassembly of the AUV and the installation of a new "fresh" power supply. In either case, the turn-around time is easily on the order of hours, dramatically limiting the fraction of time the AUV is actually in the water performing its intended mission on any given day.

1.1.4. Charging in the Marine Environment: Challenges & Benefits

Because launch and recovery is not only costly in terms of time and money but also dangerous in terms of potential for system damage and failure, it is desirable to minimize the frequency of launch and recovery. One way to do this is by installing more onboard energy storage. A larger power source allows the AUV to be on station in the water performing its mission longer. Charging is required less frequently as is launch and recovery.

Another way to minimize the frequency of launch and recovery is to somehow charge the AUV between missions in the marine environment. The benefit of this approach is two-fold. First, the AUV only needs to be launched and recovered once per set of missions. Second, the requirement to remain on station to monitor the AUV evolves; there may, in fact, no longer be a need at all to remain on station tending to the AUV. A reliable charging system might also act as a shelter for system retrieval at a later time.

Active charging might occur with the AUV underway. A surface vessel outfitted with the proper charging equipment could mate with the AUV for a short period of time and rapidly charge the AUV's power source. Inactive charging could also be accomplished with some sort of fixed or floating charging station. The second method has been attempted with some success and will be discussed in section 1.2.

The benefits of developing a robust AUV charging solution for the marine environment are many, varying from cost savings in terms of time and money to added mission flexibility and decreased logistic support requirements. Implementation, however, is not without its challenges. There are two power transfer methods available for charging an AUV power cell in the water: conduction and induction. Both methods have pros and cons, which need to be evaluated to determine which method is best for this particular application.

Conduction is the method of delivering power with which most people are familiar. It is the primary method by which household appliance receive power. Charging via conduction is characterized by a direct connection between the power source and the power cell: a plug or wire. Conduction is idea in terms of power transfer and complexity. It is near 100% efficient and requires only the weight and complexity of a plug to implement. Underwater, however, conduction becomes more challenging because the salt water must be removed from the connection site to prevent shorting and galvanic corrosion of the connectors.

Several methods have been devised to permit conduction underwater. The most common method is with the use of wet mateable connectors. While these connectors do work well, they require a considerable force and precision to effect positive engagement and disengagement. Force can be achieved with actuators. Precision is more difficult to achieve, making conduction quite difficult without the human system interaction/aid.

Inductive charge transfer is the other method of power transfer. Induction is less common than conduction. Rather than transferring power directly through a physical electrical connection, induction relies on the coupling of magnetic fields to transfer power. An alternating current flows in a primary coil, creating a time-varying magnetic field the local environment and a secondary coil (or coils) couple to the magnetic field, developing a voltage potential proportionally to the amount of magnetic flux experienced in accordance with Maxwell's equations and Faraday's Law.

Induction is safe in the marine environment, because there are no exposed electrical connections and no direct transfer of charge. As a result, there is no potential for shorting or galvanic corrosion. Power is transferred through magnetic fields only. Induction, however, tends to not be very efficient. Efficiency is a function how well the magnetic flux is coupled, and coupling is dependent upon both positional separation and alignment of the cores. Unlike conduction, power will still be transferred if the positional alignment is not perfect, but efficiency will suffer. The reduction in the need for precision is seen as an advantage for induction over conduction, despite the resulting decrease in efficiency. An AC waveform is required to generate the time-varying magnetic field required to transfer power inductively. This adds complexity to the power system design, which introduces more components and more potential for system failure. The complexity associated with an induction system is a definite drawback to this method of charging.

1.2. Previous Work with AUV Charging in the Marine Environment

A lot of work of work has been done by a number of different research labs and commercial companies to develop underwater AUV charging docks. Methods vary, and success has been incrementally improved over the years. A review of the most recent docking stations and methods is provided in the following sections. A chronology is followed; the most recent systems are discussed last.

1.2.1. AOSN Dock

One of the first attempts to dock and recharge an AUV was the Autonomous Ocean Sampling Network (AOSN) docking system. Designed specifically for the MIT Odyssey II AUV, the AOCN dock provides a recharging and data transfer capability. Charging is accomplished via induction, with a receiver core mounted under the nose of the AUV [7]. The system is quite complex, relying on a mooring system and a latching mechanism, illustrated in Figure 3.

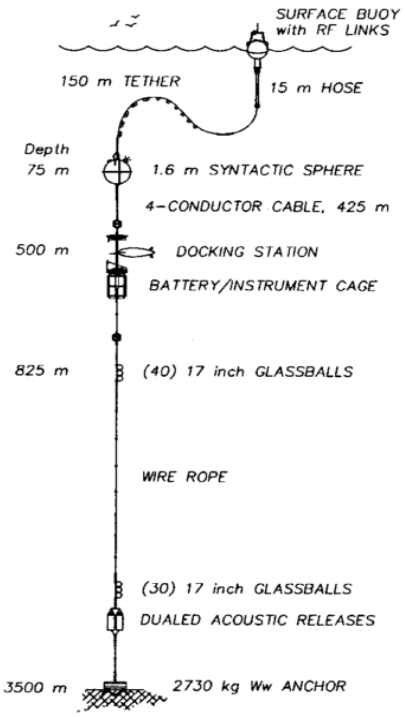

Figure 3: AOSN Docking System for the MIT Odyssey II AUV [7]

The AOSN docking system was fielding in 1998 as a joint venture between MIT SEA GRANT and Woods Hole Oceanographic Institute (WHOI) in the Labrador Sea with marginal success. The details of the system are discussed in [7]. Most of the issues with the system stemmed from the use of a "scissor" latching mechanism on the nose of the AUV. Positive engagement of the AUV to the mooring tether required the latching mechanism to catch the tether in a dynamic ocean environment. The AUV was then winched down the battery/instrument cage for recharging and data download [8]. When positive engagement of the AUV was achieved, power transfer was at approximately 80% efficient – a promising result for inductive power transfer. Deployment and recovery of the system, however, was difficult requiring almost a full day in moderate sea conditions to accomplish.

1.2.2. MIT AUV Recharging System

A variation of the AOSN docking system was designed and lab tested at MIT Sea Grant by L.A. Gish in 2004 [9]. Again induction was pursued, but with a slight variation. Rather than align the induction coils with the mechanically unreliable winch system featured in the AOSN dock, the tether itself could be used for power transfer. The idea was based on a common mining practice in which Linear Coaxially Wound Transformer (LCWT) are used to transfer power to mining machinery directly from a loop of wire in which AC is flowing. A LCWT coil built into the latching mechanism of the AUV could be used to inductively transfer power for recharging immediately upon positive engagement of the latch. The envisioned system is illustrated in Figure 4. The loop of wire coaxial cable is suspended in the water column by a buoy, which provided both stiffness and damping to the system to permit latch engagement.

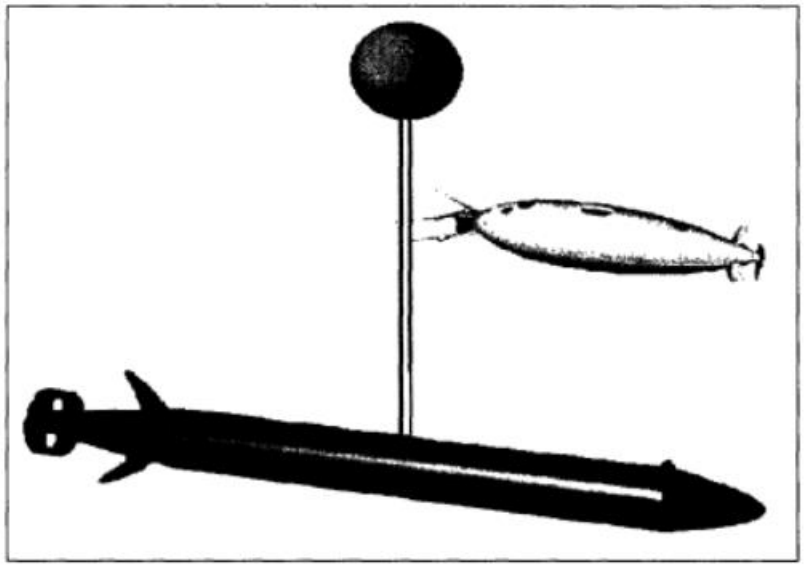

Figure 4: AUV Recharging System using LCWT [9]

Lab tests of the prototype system provided poor efficiency results. Marine environment testing later conducted on the system in conjunction with WHOI and MIT SEA GRANT found latching too difficult and unreliable in actual marine environment to continue pursuing. While this system might hold promise for future research and application, no additional data is currently available on any other tethered LCWT systems.

1.2.3. REMUS 600 Dock

Hydroid, a commercial company owned by Kongsberg Maritime, has been producing the popular REMUS series of AUVs for several year. WHOI fielded a prototype docking station for the REMUS 100 AUV in 2001 [10]. This prototype docking station sought to remove the AUV from the dynamic nature of the ocean environment by providing a cylindrical housing enclosure. The AUV was driven into a cylindrical tube and mechanically retained prior to the initiation of power transfer or data download. A graphic of the prototype is provided in Figure 5.

The most interesting innovation of this docking system is the use of a "docking cone." The cone helps minimize the level of precision required to dock the AUV by increasing the target size. The AUV approaches the entrance to the cylinder. Misalignments are corrected for mechanically through the use of the cone. Other issues complicate the approach. Specifically the AUV must orient itself to the entrance, which is another engineering problem altogether.

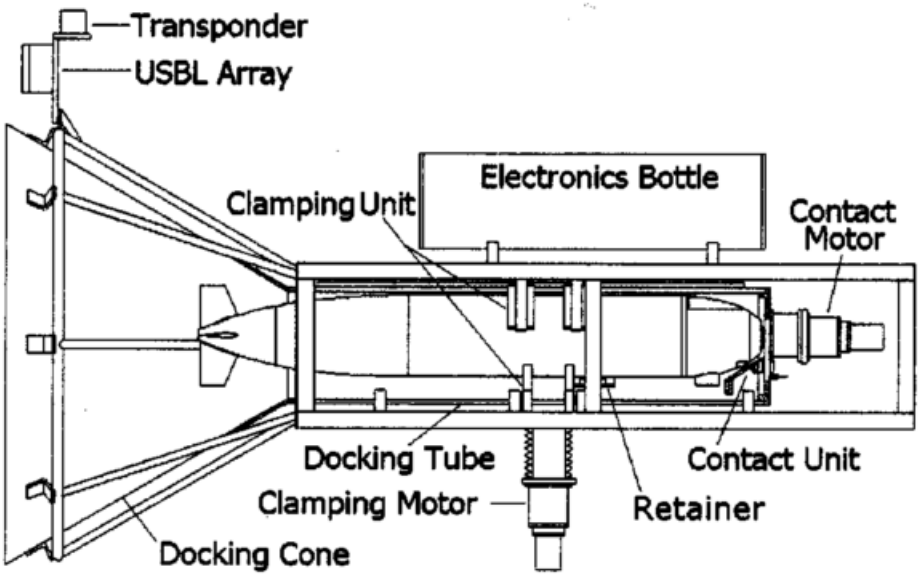

Figure 5: REMUS 100 Docking Stations developed by WHOI. Fielded 2001 [10]

Once inside the cylinder with the retainer positively engaged, the docking station would clamp down on the AUV and initiate the charging and data collection sequences. The dock featured inductive charging and data transfer using specially shaped transmit and receive cores configuration which maximized coupling [11]. The system was 70-83% efficient during operational tests and is shown in Figure 6. The interesting aspects of this particular system include the "hockey puck" coupling design of the induction coils. Transmit and receive coils are inlayed into the two pucks. The transmit puck is mechanically driven into the receiver puck. Positive mating is ensured by the geometry of the system. To properly mate, the transmit coil must fit perfectly into the provided indentation. The slope of the sides of the indentation enable mating to occur relatively easily with an appropriate amount of mechanical force, despite slight misalignments that may exist in initial positioning.

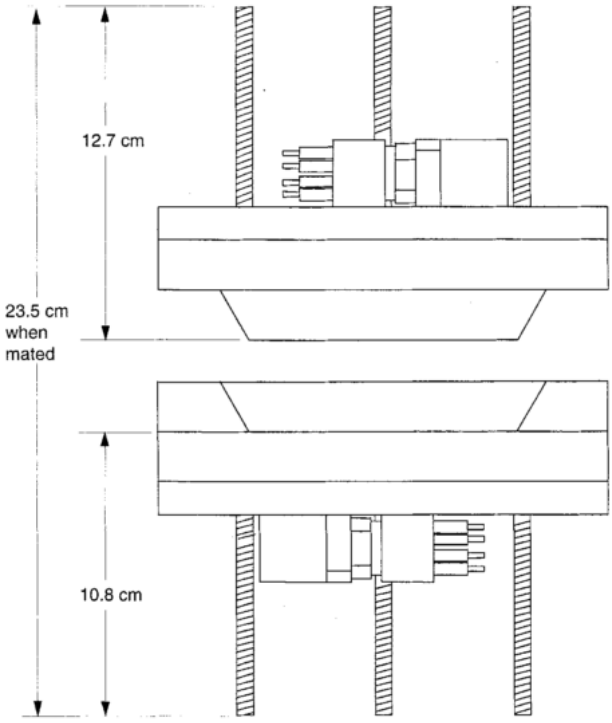

Figure 6: Transmit and Receive Core Assembly for Power and Data Transfer [11]

Several modifications were made the original docking model to improve system performance and reliability. In 2006, WHOI experimented with a second generation dock based shown Figure 7. The most immediate difference observed is the shape of the docking cone. It is square rather than circular.

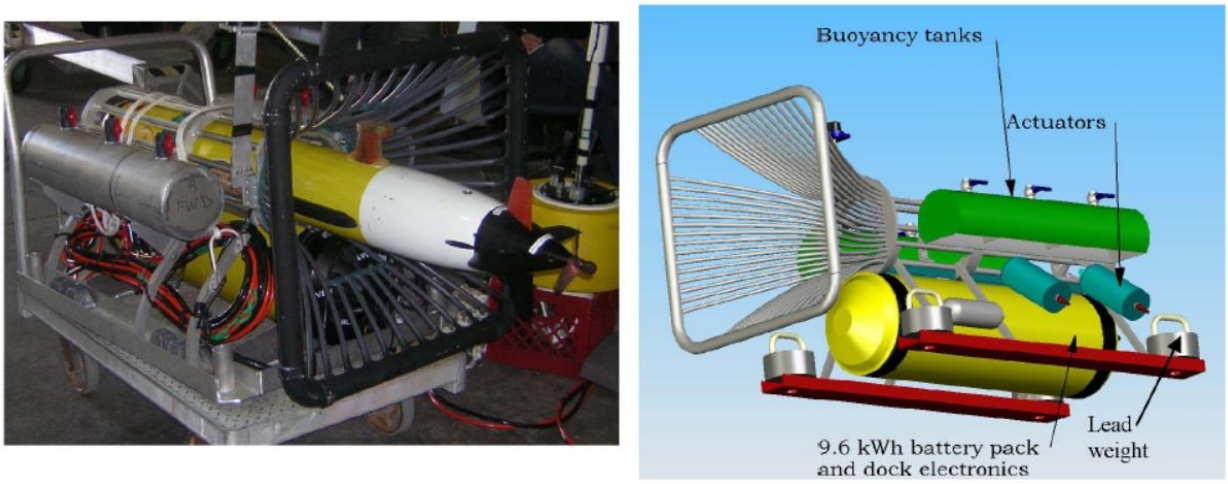

Figure 7: Hydroid REMUS 100 Docking Stations fielded 2006

Much more important operational changes were made in this dock though. First, power and data transfer were decoupled; they occur independently. Data is transferred with the use of an optical modem. And power transfer is not accomplished inductively. WHOI observed excessive bio-fouling of the contact surfaces in the first generation prototype. To correct the problem, the inductive coupling

core system of Figure 6 was replaced with a guide pin, single power connector stab system shown in Figure 8. This conduction system increased efficient to nearly 100% and increase system reliability. This system is the current design for REMUS 100 docks being deployed by WHOI for research purposes. Hydroid also tests and sells a similar dock based on the same design and technology [12].

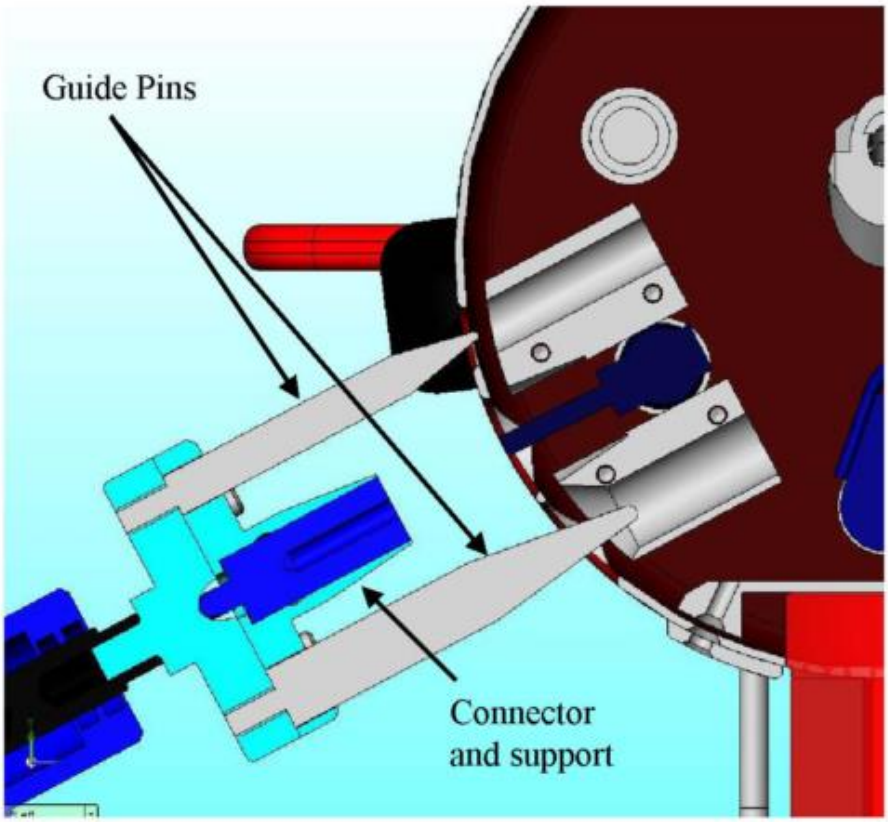

Figure 8: Dual Stab, Single Connector Power Transfer System on REMUS 100 Docking Station

1.2.4. Bluefin 21 Dock

Hydroid is not alone in its efforts to find a docking station for its AUVs. Bluefin Robotics, another manufacturer of world-class AUVs, has also developed proprietary docking stations for its much larger 21" diameter Bluefin-21 AUVs. The concept of operation, however, is varied little from those developed by WHOI and Hydroid. A docking cone is used to guide the AUV into a cylindrical retaining tube in which power and data transfer are accomplished [13]. The docking station was developed in collaboration with Battelle[14] and is shown in Figure 9

Figure 9: Battelle-developed Docking Station for Bluefin 21 AUV

The Battelle solution is unique in that the docks can be stacked and joined together to form docking modules permitting the docking of any number of AUVs at a given time. Separation of cells is performed using acoustic beckon signal at the entrance to each dock. Additionally the dock and AUV can be deployed together. The entire system is lowered to the seafloor. The AUV then drives out of the dock and returns when its mission is complete or power is needed.

The US Navy has expressed interest in this particular solution as a means of rapidly delivering a payload and/or capability as needed. The system can also be deployed and lay in wait for long periods of time until it is needed.

1.2.5. Docking/Charging Station Issues

The docking station does not come without its challenges. First, bio-fouling of sensors and components is a real concern, as previously mentioned in 1.2.3. Optical sensors and induction coils do not work well when covered in marine growth. Consequently, these docking stations are maintenance intensive solutions that prolong AUV deployment, but not indefinitely. The docks can stay in the water for several weeks, but reliability decreases if the system is not cleaned regularly. It might be possible to automate the cleaning of these docks and increase their viability over the long run. This problem and its possible solutions are not addressed here and is an area for future research.

Second, the docks currently are designed to carry a single recharging battery pack. Once the AUV is recharged once or twice, the charging station much be brought to the surface and recharged itself. Some ideas have been discussed with the US Navy to develop an energy harvesting capability that would remove power as a limiting factor. Energy could potentially be harvested from wave action or some other means locally. This is an area for future research and exploration.

Finally, the AUVs are limited in navigational intelligence. Occasionally, the AUV fails to enter the dock. As sensing algorithms and artificial intelligence of these systems increase, their reliability will also increase. At this time, however, coupling sensor degradation due to bio-fouling with the need to provide high-precision underwater navigational sensing guidance is a challenge that will need to be addressed and solved before wide-spread, long-duration deployment of these systems can be accomplished.

1.3. Proposed System Overview

The charging system is comprised of three separate components. First, there is the power source. The source includes both the power supply and the inductive coils. The power converter is the second component. The final component is the battery pack. A system overview is shown in Figure 10.

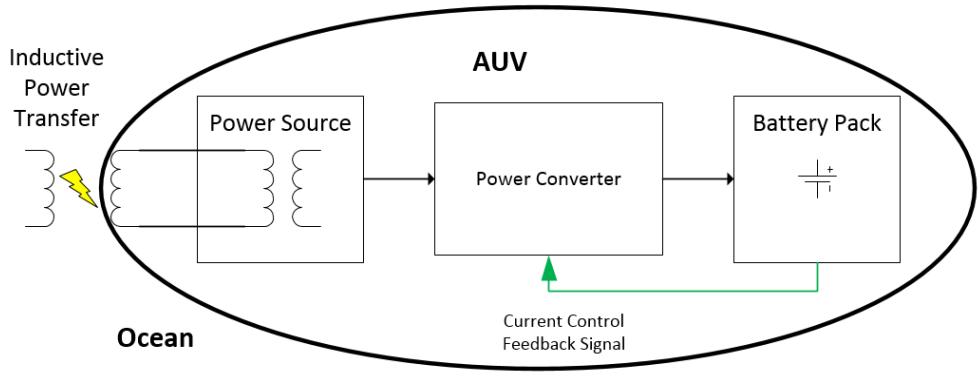

Figure 10: Power System Overview

The objective of this thesis was to design and to build the power converter block. Focusing on the power converter required successfully decoupling it from the rest of the system. By properly characterizing an interface between the power source and power converter, a separate power source was interfaced for testing and evaluation of the converter. Similarly, the battery pack was replaced with a set of design specifications and replaced with a resistive load for testing.

1.3.1. Battery Pack Specifications

The AUV battery pack for this project was a known design constraint. Each pack will consist of 12 A123 ANR26650M1-B Nanophosphate® High Power Lithium Ion (Li-Ion) Cells. These cells will be arranged in series with a nominal cell voltage of 3.3V [15]. Cell voltage, however, can and will vary between 3.7V and 3.3V. A quick calculation provides the first specification for the power converter: output voltage. Output voltage is expected to vary between 39.6V and 44.4V.

These cells are capable of fast-charging at 10A. Charging AUVs in the water presents unique challenges for the charging evolution. On dry land, charging can be completed over long periods of time and under calm conditions. At sea, however, if the AUV is to remain in the water during the charging evolution, charging as fast possible is desirable. Fast charging minimizes the amount of time the power source must be close proximity with the AUV while maximizing the useful mission time of the AUV. The desire to conduct fast-charging of these cells at 10A provides the second power converter specification.

The desired output power of the system is calculated as follows:

$$P_{out} = I_{out}V_{out,max} = 10A * 44.4V = 440W$$

To account for efficiencies and provide some engineering margin to the final design, the system was built for a design limit output power of 500W.

1.3.2. Power Source Specifications

The power source will almost certainly be a diesel generator connected to an inductive coil set. The coil set for power transfer to the AUV from the surface power source is still in the design phase of production. Per power converter, however, the power source will need to be able to supply 500W of real power plus a 10% loss margin for a total input power of 550W. An assumption was made in the design process that the required power will be available and will be transferred at high voltage, low current.

A marine diesel generator would be an ideal power source, because a large amount of power would be required to charge multiple battery cells as once. If 10 cells are charged simultaneously, which is highly likely for a fielded system, 5.5kW of power would need to be provided. A small marine diesel generator mounted onboard a surface vessel or platform would be idea for such an application.

To minimize the amount of copper required for power transfer and the I^2R losses associated with the supply cabling, a high voltage, low current AC input power is expected. A low voltage, high current option would increase the size and weight of the power source cabling and decrease overall system efficiency. This is a standard practice for the transfer of large amounts of power.

Figure 10 shows a transformer in the Power Source block. Power is supplied from the unspecified AC source described and transmitted through an input transformer. The input transformer depicted in Figure 10 serves to decouple the power source from the power converter. For the final system, any transformer that provides the correct output AC voltage can be used. Any frequency within the rating of the rectifier is appropriate. The AC waveform is first rectified, then filtered and conditioned.

The ideal power source for testing is any AC source capable of supplying at least 550W. A North American standard 120VAC electrical supply outlet was chosen for convenience. It can source 550W and is protected with breakers in all residential and industrial facilities.

1.3.3. Power Converter Specifications

Defining the specifications for the power source and battery pack permit the proper specification of the power converter. The high input voltage suggests the use of a non-isolated step-down (buck) converter. However, even if the input is not high voltage, low current, an appropriate input transformer can be selected to adjust the input voltage to an acceptable operating range, permitting the use of a buck converter.

A buck converter topology is not the only option that could have been chosen. Numerous switching mode power supply (SMPS) topologies exist that would have acceptable for the application described herein. The buck converter topology was chosen for a few basic engineering reasons:

1) Efficiency – An SMPS is needed to ensure an acceptable level of system efficiency. A linear regulator would have resulted in an unacceptably low efficiency, heat management problems, and poor transient response behavior.
2) Flexibility – The buck converter, as with all SMPS solutions, uses Pulse Width Modulation (PWM) to adjust the duty cycle. PWM adds flexibility to the design by allowing the output voltage and current to vary as a function of duty cycle, which can be actively controlled.

3) Simplicity of Design – The buck is a widely used, well-understood SMPS topology with few components. Its simplicity is attractive for the AUV environment, where volume restrictions make larger, more complex solutions less desirable.
4) Reliability – The traditional buck topology has high reliability, because it has only one actively-controlled switch. All other components are passive. On an AUV, reliability is required to prevent asset loss.
5) Constant Output Current – For a given duty cycle, the buck converter features a constant output voltage proportional to the duty cycle and, therefore, a constant output current. Current is desired to be as constant as possible for battery charging. The Ćuk and Zeta topologies also provide a constant output current but feature a much higher, unnecessary level of complexity [16].

The need to regulate the output and provide 10A suggests the need for some form of feedback. Feedback design specifics will be covered later. The rest of the specifications are functions of design constraints and customer desires. At the onset of the design process, the specifications outlined in Table 1 where developed with input from the power source and battery pack designers.

Table 1: Buck Converter Requirements & Specifications

REQUIREMENT	SPECIFICATION
Input Voltage Range	60 -75 VAC
Input Voltage Transient Limit	80VAC for up to 1ms
Output Power Range (Resistive Load)	500W
Output Voltage	39.6-44.4VDC
Output Current Transient	Never > 14A 12A+ for < 0.5ms
Output Voltage Ripple	5mV or less
Input Current Ripple	100mA
Min Efficiency	90%
Ambient Temp Range	-20°C to 25°C

There was a drive to ensure that the system as a whole was compact. It needed to fit inside an AUV. Space is a valuable commodity onboard these vessels. Therefore, the onboard power system must be both compact and reliable. The buck converter was chosen because it offers both compactness and reliability. Size will be discussed in greater detail when PCB layout is reviewed.

2. Converter Design

The power converter was designed with all the system specification outlined in the Proposed System Overview close at hand. The decision to design a buck converter with feedback was the result of two factors. First, the system needed to charge a battery pack. Batteries are DC components that required DC current for charging. Second, the design team pinned the converter input voltage requirement to 60-75VDC, resulting in the need for a DC-DC power converter topology.

Determining the output voltage required knowing the effective series resistance (ESR) of the battery pack. Each battery cell has a 6mΩ ESR for a total pack ESR of 76mΩ [15]. A small pack resistance translates to the ability to drive large amounts of current at a relatively small voltage potential. With a pack voltage of approximately 44.5VDC max, the output voltage need not be much more than 45VDC to drive the required 10A of output current. The output voltage is therefore lower than the input. A buck converter is required.

2.1. Buck Converter Theory

A buck converter is a DC-DC power converter than takes a high voltage input and converts it to a lower voltage output through switching action. An ideal buck converter transfers power from input to output without losses. Real converters lose power in the form of heat in both switches as well as the inductor. Figure 11 shows a basic buck topology.

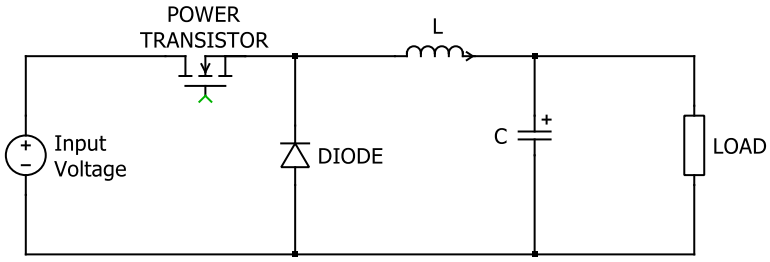

Figure 11: Basic Buck Converter Topology

The buck converts functions by swapping conduction between two power switches. In Figure 10, the two switches are the power transistor and the diode. When the transistor is conducting, the diode is off and the output inductor L builds current, storing energy in its magnetic field. When the transistor if off, the inductor L dissipates energy stored in its magnetic field to turn on the diode and continue driving current to the load.

The power transfer process starts with the first switch: the power transistor. A control signal turns the transistor "on." It conducts and transfers the input voltage to the load through the inductor L. The inductor builds up current and stores energy in its magnetic field during this stage. The control signal then turns the transistor "off" for the second part of the operational cycle. The input voltage is isolated from the load, but the current flowing in L cannot instantaneously change. Energy stored in the magnetic field of L continues to drive current to the load, inducing a negative voltage across the freewheeling diode. The diode turns "on" and permits current to be delivered to the load. L and C act as a second order filter to smooth the output waveform. The load experiences an average voltage proportional to the fraction of the transistor's per cycle "on" time. Depending on how long the transistor is on per cycle, more or less power is delivered. The ratio of the "on" time to total cycle time

is called the duty cycle D. For a buck converter, the relationship between duty cycle D to input and output voltage is:

$$V_{out} = D\, V_{in}$$

While a complete description of exactly how the buck converter operates is not provided, it is sufficient to say that the buck converter is a DC-DC converter topology that reduces input voltage proportional to its duty cycle. A complete theoretical description of how a buck converter operates is provided in Principles of Power Electronics [17].

Operational detail for the selected design will be provided as this chapter progresses.

2.2. Power Converter Design Overview

The simple buck converter illustrated in Figure 11 was not sufficient for the AUV charging circuit, because the actual input is not a DC power supply at all, but an AC waveform that must be transformed, rectified, and filtered to approximate DC. Additionally, input filtering and output filtering was required to ensure an acceptably smooth current waveform was delivered to the battery at all times. The actual designed converter topology is shown in Figure 12.

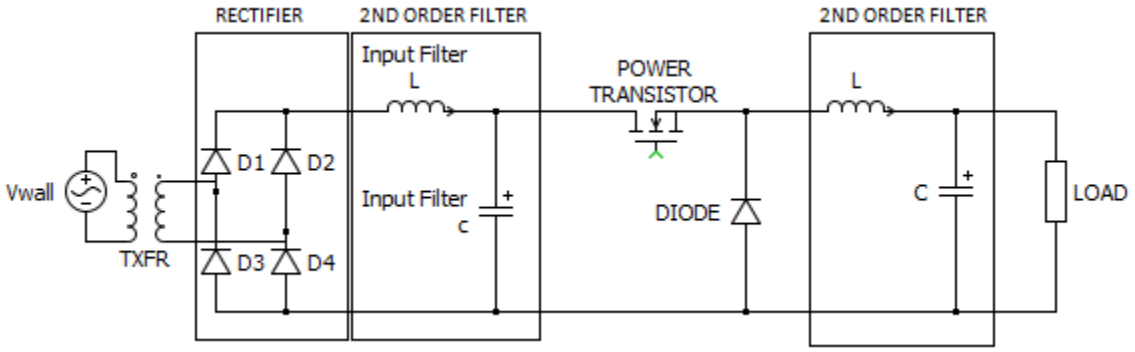

Figure 12: Buck Converter Topology for AUV Charging System

Using a transformer at the frontend of this converter permits a much higher level of flexibility with this design than might otherwise be present. A much wider range of AC sources with sufficient power throughput can be coupled to this system with the right transformer. The transformer also effectively provided isolation for each individual battery pack from the power source, preventing a potential fault or failure in one charging circuit from affecting another during the charging cycle.

2.3. Switching Frequency Selection

In general, higher switching frequencies are preferred for power converters as they permit the use of smaller (and usually cheaper) inductors and capacitors – both for filtering and power conversion [18]. Smaller passive components translate to smaller board and volume requirements and more compact designed. Compactness is ultimately the driver for using a higher switching frequency is this application. Volume onboard an AUV is valuable and limited. The recharging system cannot be allowed to monopoly vital volume needed for useful sensor payloads, like sonar and acoustic modems.

The switching frequency for any application cannot be increased to an arbitrarily high value. Several physically limitations exist preventing excessively fast switching. First, the power transistor can only switch so fast. Second, passive components are required to allow a buck converter to function properly. The capacitors and inductors cannot be engineered out the design with an unreasonably fast frequency [18].

High switching frequencies buy smaller component sizes, faster transient response, and small voltage over and undershoots at the expense of efficiency [18][19]. Lower efficiency drives an increase in the heat load of the system, which must be dissipated and dealt with appropriately. Often the need to remove heat can again increase the size of the system.

A comparison between switching frequency and efficiency for a nominal DC/DC converter was done in an EE Times article titled, "Choosing the optimum switching frequency of your DC/DC converter" [18]. The specification of the converter are not important. Varying only switching frequency for a given DC/DC converter design, the effect on efficiency would be the same as that shown in Figure 13. The efficiency of the entire system suffers across the entire spectrum of loading conditions [19].

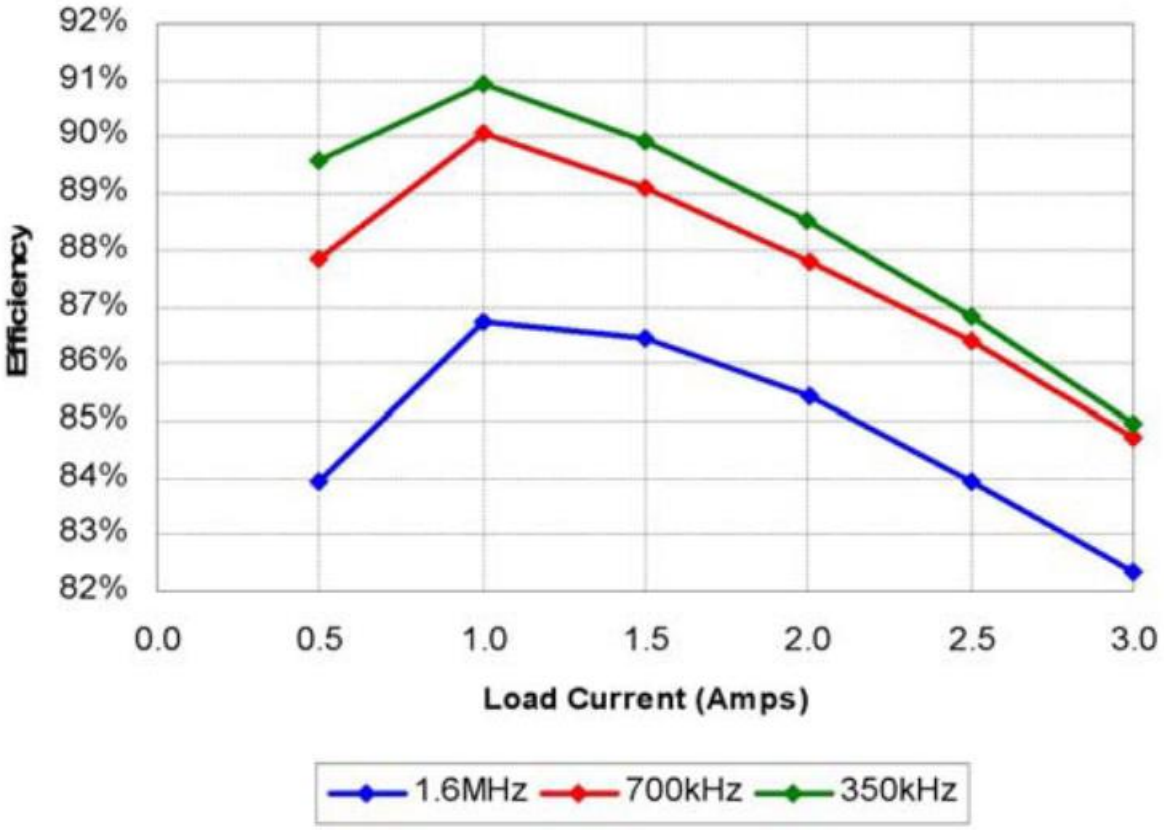

Figure 13: Efficiency vs. Switching Frequency at Various Loading States of a Nominal DC/DC Converter [18]

In this design, the switching frequency was limited by the required efficiency of the converter and the availability of acceptable power components.

In other words, an arbitrary switching frequency cannot be chosen because at some point efficiency will become unacceptable due to losses in the switches (capacitive charging losses in the diode and

conduction and switching losses in the MOSFET) and inductors (I^2R and coil losses). These loss mechanisms increase proportional to frequency, though the switching losses of the MOSFET have the greatest effect on overall system efficiency as frequency increase [20].

For this design, 600kHz was chosen for switching frequency f_{sw}. This frequency represents a good trade-off between moderates small component sizes and acceptable power converter efficiency.

2.4. Switch Selection: Power Diode

The diode was the first power electronics switch selected in the design process. From the requirements, the diode will need to be able to withstand a maximum input voltage of 80V for 1ms. This requirement captures the need to protect the diode during transient load changes during which the voltage across the device can spike. The diode must also be able to withstand the maximum current it is likely to experience during regular operation. A calculation is required to determine the steady-state maximum diode current $< I_{diode,max} >$.

To find $< I_{diode,max} >$, first the maximum output current $I_{out,max}$ must be determined.

$$I_{out,max} = \frac{P_{out,max}}{V_{out,min}}$$

Maximum output power $P_{out,max}$ is a function of the required output voltage and the output current. Maximum voltage for each cell is 3.7V for a total pack voltage of 44.4V. The desired average output current is 10A, with an $I_{out,max}$ of 10.5A maximum. Accounting for efficiency, we estimate $P_{out,max}$ to be 500W.

$V_{out,min}$ is directly related to the minimum voltage of the battery pack. For this calculation, we will take the minimum voltage of each battery as the nominal voltage of 3.3V. The pack consists of 12 battery.

$$I_{out,max} = \frac{500W}{12 * 3.3V} = 12.62A$$

This is the maximum current, not the average. The duty ratio needs to be determined to find the average. For a BUCK CONVERTER,

$$V_{out} = D\, V_{in}$$

V_{in} ranges from 75-60V, and V_{out} is nominally 45V to supply the required 10A. Therefore, the duty cycle D is expected to ranges from 0.6 to 0.75.

$$D = \{0.6, 0.75\}$$

$< I_{diode,max} >$ can now be calculated as:

$$< I_{diode,max} >= I_{out,max}\,(1 - D_{min}) = 12.62A(1 - 0.6) = \ 5.05A$$

The Vishay Dale V12P10 Schottky Rectifier was chose as the diode for this application. The device is rated for a maximum average forward current of 12A with a peak surge current of up to 200A for 10ms. Additionally the device is surface mount and offers the unique ability to dissipate heat directly to the PCB. This feat will be discussed when heatsink calculations are presented.

2.5. Switch Selection: Power Transistor

The second power switch that needed to be characterized and selected was the actively controlled power transistor. For this application, an N-Channel MOSFET switch was chosen. Other options were explored, including IGBTs. The 600kHz switching frequency f_{sw}, however, made IGBTs an undesirable technology for this application.

Similar to the diode, the MOSFET needed to be rated to withstand the maximum input voltage transient of 80V for 1ms and to handle the maximum average MOSFET current $< I_{FET,max} >$. It will also need to be as efficient as possible to prevent exceeding the desired 90% efficiency.

The calculation for $< I_{FET,max} >$ assumes the worst case efficiency, lowest input voltage, and highest duty ratio.

$$< I_{FET,max} >= \frac{P_{out,max}}{\eta * V_{in,min}} * D_{max} = \frac{500W}{0.90 * 60V} * 0.75 = \ 6.94A$$

6.94A is the most steady-state average current the MOSFET will experience during normal operation.

From this information, the International Rectifier IRL520NPBF was chosen. It is rated for a minimum of 500V drain-to-source voltage, can handle up to 10A continuous, with a pulsed source-to-drain current of 35A. A better candidate in terms of power loss and overall efficiency probably exists. For the purposes of proof-of-concept and prototyping, however, the IRL520NPBF is more than adequate for the AUV charging circuit.

2.6. Input Filter Passive Component Selection

A 2nd order LC low-pass filter is required for block high frequency components of the input power. The parallel LC tank depicted in Figure 14 forms the foundation of the input low-pass filter design. The additional impedance Z3 is known as R_d-C_d parallel damping. Parallel damping was introduced into the design to provide damping at the filter's resonance frequency, $\omega_o = \frac{1}{\sqrt{L_f C_f}}$. R_d provides the required damping resistance, while C_d is a large DC current blocking capacitor used to prevent excessive power loss. C_d should be large enough such that its impedance $\left(\frac{1}{j\omega C_d}\right)$ is negligible compared to R_d at the resonance frequency.

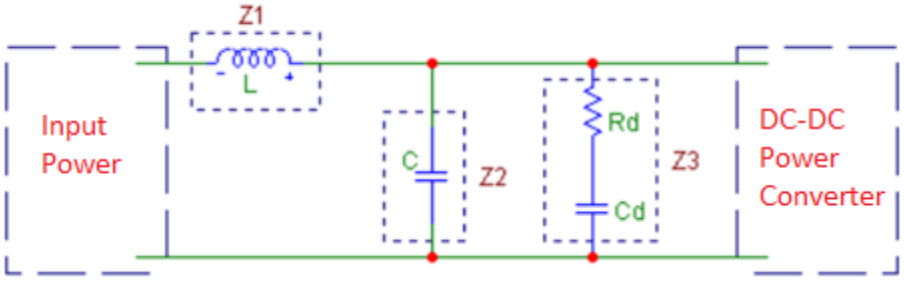

Figure 14: Input Filter to Buck Converter Switching Components

The transfer function of this filter is not trivial to derive. It is, however, determined by the Laplace transform and calculated as follows [21]:

$$\frac{i_{in}(s)}{i_{out}(s)} = \frac{Z_2||Z_3}{Z_1 + Z_2||Z_3} = \frac{1 + sR_dC_d}{1 + s^3LCC_dR_d + s^2L(C + C_d) + sR_dC_d}$$

The addition of parallel damping significantly improves the low-pass filter performance at resonance. Figure 15 shows an illustration provided by a National Semiconductor Corporation application note that clearly illustrates the expected performance of this type of filter [21]. The red line plots the expected undamped filter transfer function response. The dotted blue line plots the damped response. The important takeaway from Figure 15 is that the peaking at resonance is effectively nullified, and filter performance is much improved. Figure 15 also shows the expected -40dB/decade past the cutoff frequency, which verifies the performance attributes of the filter. It passes frequencies less than the cutoff frequency with little to no attenuation, and sharply attenuates frequencies higher than cutoff.

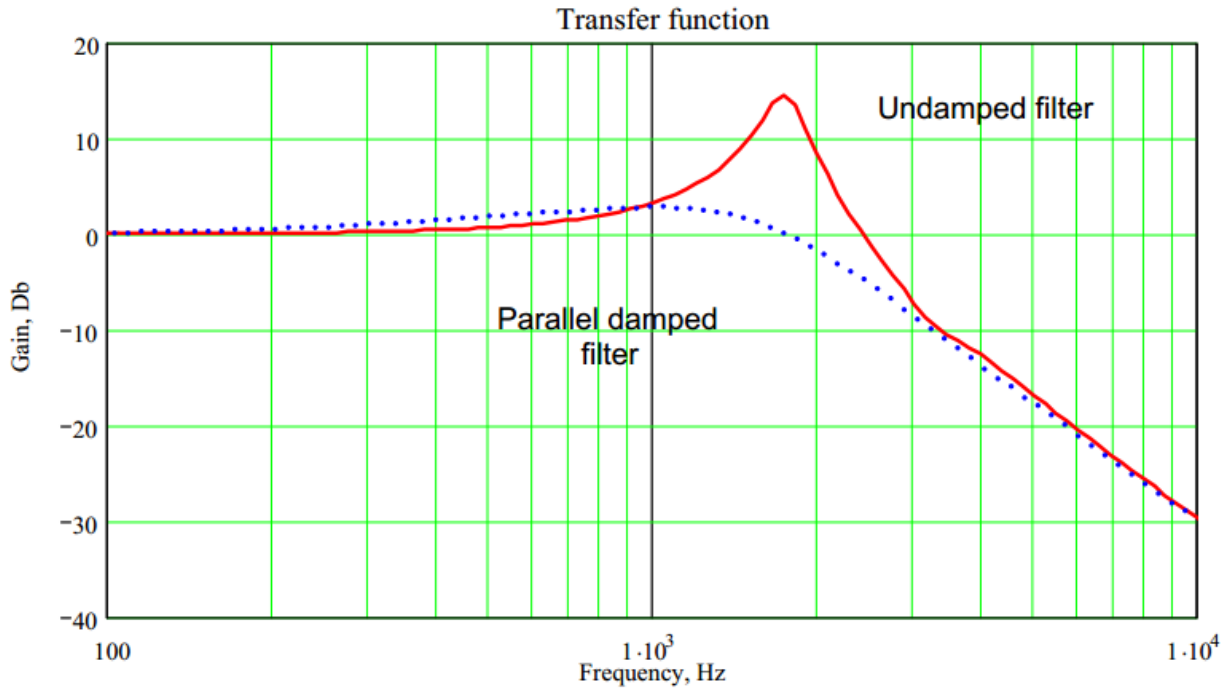

Figure 15: Transfer Function Response of Parallel Damped vs. Undamped Low-Pass Filter

The LC constant of the low pass filter is now chosen to attenuate the input current ripple to the desired level of less than 100mA. Current without the filter is determined from the fundamental of the current waveform at the input to the drain of the MOSFET. The worst case input current ripple fundamental is calculated as:

$$i_{in,fund}^{pk-pk} = \frac{4}{\pi} * \frac{P_{out,max}}{\eta V_{in,min}} * D_{max} = \frac{4}{\pi} * \frac{500W}{.90 * 60V} * 0.75 = 7.07A$$

The output current ripple is also solved for completeness.

$$i_{out,fund}^{pk-pk} = \frac{4}{\pi} * \frac{P_{out,max}}{\eta V_{out,min}} * D_{max} = \frac{4}{\pi} * \frac{500W}{.90 * 39.6V} * 0.75 = 13.40A$$

This filter design must ensure that a 100mA input current ripple is not exceeded. The required dB attenuation necessary to accomplish this design object was calculated as:

$$dB = 20\log\left(\frac{i_{in,fund}^{pk-pk}}{100mA}\right) = 20\log\left(\frac{7.07}{.1}\right) = 37\ dB$$

The cutoff frequency f_{co} was complicated to assess in this case. The MOSFET switching frequency is 600kHz, the North American standard 120VAC electrical outlet is a standard 60Hz, and the final power source will probably on the order of 1MHz. 1MHz is based on on-going research being conducted at MIT SEAGRANT, which has shown promising inductive power coupling results in this frequency range. Tuning of the coupling circuit is required to achieve a high quality factor Q and effective power transfer over a range of vertical and horizontal distances and orientations, but the target frequency range is 1MHz ± 20%.

The 60Hz input frequency for testing, which is rectified to 120Hz, is all but impractical to completely filter out, so a design decision was made to tailor the solution to the final application vice the test condition. A cutoff frequency f_{co} of 50 kHz was therefore chosen. A 50kHz cutoff frequency will effectively eliminate all frequencies greater than 500kHz (one decade higher than cutoff) from the input. This means that minimal changes will be required for integration of the final design into the AUV. It also means, unfortunately, that the 60Hz frequency of the electrical outlet will not be filtered by the input filter. Smoothing and filtering of the input voltage will have to be accomplished with an input rectifier network and smoothing capacitors.

The relationship between the cutoff frequency, the input filter inductor L, and the input filter capacitor C is:

$$\omega_o = 2\pi * f_{co} = 2\pi * 50\text{kHz} = 314159\ {}^{rad}/_{sec} = \frac{1}{\sqrt{LC}}$$

Using this relationship, L and C must to be chosen to provide the desired filtering. For convenience, L was chosen first to be 1µH. Solving the equation for C yields:

$$C = 10\mu F$$

The Vishay Dale IHLP3232DZER1R0M11 1µH surface mount inductor was selected for L. It is rated for a maximum peak current 18.2A. A TDK Corporation 10µF ceramic capacitor was chosen for C. A ceramic capacitor was used because ceramic offers high stability and low losses over a wide range of frequencies.

The selection of C_d was driven by a balance between the sizing of R_d and C_d. C_d should be large enough such that its impedance $\left(\frac{1}{j\omega C_d}\right)$ is negligible compared to R_d at the resonance frequency ω_o. This is done to ensure that the R_d-C_d parallel damping shunt looks resistive at resonance, allowing it to damp as expected. Effective damping also requires $C_d \gg C$.

Because the circuitry is intended to be housed in the open pressure housing of the AUV, a Panasonic 80V 1000µF aluminum electrolytic capacitor was chosen for C_d. The impedance of C_d at resonance is approximately 3.2mΩ. Electrolytic capacitors would be an unacceptable capacitor selection for a system requiring pressure compensation due to its internal construction. The system being designed in

intended to be housed inside the pressure housing of the AUV. Electrolytic capacitors are therefore considered acceptable and have been selected for the design. This design decision can be reevaluated as needed during future development.

To properly size R_d, two requirements derived from examining the input impedance (Z_{in}) and the output impedance (Z_{out}) much be met. First, R_d must be less than Z_{in} to ensure damping. The incremental impedance of the power converter about an operating point is given by:

$$R_d \ll Z_{in} = \frac{dv_{in}}{di_{in}}\bigg|_{op\ point} = \frac{-P_{out}}{I_{in}^2}$$

The calculation shows that the converter actually looks like a negative resistance about an operating point, which is a destabilizing attribute. To ensure the system remains well damped despite the tendency of the negative input impedance (Z_{in}) to undamped the system, the effect of R_d in parallel with Z_{in} must be considered.

$$R_d||Z_{in} = \frac{-R_d\left(\frac{P_{out}}{I_{in}^2}\right)}{R_d - \frac{P_{out}}{I_{in}^2}}$$

The numerator is negative. To ensure the combined resistance offered by the network is positive, the denominator must also be negative:

$$R_d - \frac{P_{out}}{I_{in}^2} \ll 0 \qquad \text{->} \qquad R_d \ll \frac{P_{out}}{I_{in}^2} = \frac{500W}{7.1A^2} = 9.9\Omega$$

R_d must be much less than approximately 10Ω to meet ensure positive resistance is experienced by the circuit at resonance.

The filter will also be damped only if R_d is less than or equal to Z_{out}.

$$R_d \leq Z_{out} \qquad \text{, where } Z_{out} = \sqrt{\frac{L}{C}} = \sqrt{\frac{1}{10}} = 0.32\Omega$$

A 0.3Ω 1W 5% axial resistor was chosen for this application based on the calculations provided.

2.7. Output Filter Passive Component Selection

The output filter for the buck converter is also a 2nd order LC system. The need for output filtering stems from the desire to provide the cleanest DC signals possible to the battery pack during the charging evolution. The selected batteries can handle some level of voltage and current fluctuation, but not much. That is why the output voltage ripple specification is so tight (<5mV). No damping is provided in the output filter, as seen in Figure 33.

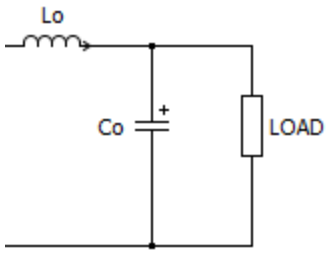

Figure 16: Output Filter Circuit

To properly size the output inductor L_0, the peak-to-peak inductor current ripple i_{out}^{pk-pk} must be calculated.

$$i_{out}^{pk-pk} = \frac{1}{2}\frac{V_{in}}{L_o}\frac{T}{2}$$

, where L_o is the required output inductance and T is the switching period. The design requirement, however, was set to limit output voltage ripple to 5mV. This will ensure that the current ripple to the battery remains within acceptable limits, which is what we care about for our constant current charging application. Peak-to-peak output voltage v_{out}^{pk-pk} is calculated as:

$$v_{out}^{pk-pk} = \frac{1}{2}\frac{1}{C_o}\frac{i_{out}^{pk-pk}}{2}\frac{T}{2} = \frac{1}{32}\frac{V_{in}T^2}{C_oL_o} \leq 5mV$$

, where C_o is the output capacitance.

Noting that the worst case output voltage ripple occurs at max input voltage,

$$C_oL_o = \frac{1}{32(5mV)}(75V)\left(\frac{1}{600kHz}\right)^2 = (1.30 * 10^{-9})FH$$

Now a design decision is needed to pick an appropriate inductor/capacitor mix. Inductors are large and costly, in general. To keep costs down and to simply the design, most of the passive component requirement for output filtering will be satisfied by capacitors. Also, a large aluminum electrolytic capacitor will be used in conjunction with smaller ceramic capacitors to increase the performance of the filter.

L_o was chosen to be 15µH. This was a convenient inductor rating that could be found for surface mount application. With L fixed,

$$C_o \cong 90\mu F$$

30µF was allocated to ceramic capacitors. A 100µF aluminum electrolytic was used for provide the remaining capacitance. This is more than was required, but 100µF electrolytic capacitors are readily available in a wide range of voltage ratings and will improve the performance of the final product.

Output current ripple can also be calculated at this point. Worst case output current ripple on the induction is 2.08A. Because the output current is so high, the inductor will take time to build up charge. When designing the feedback, the lag-time of the output inductor needs to be kept in mind. The

feedback ci at which point it will switch to continuous-discharge operation and operate as expected for this application. The current selector presented represents a good balance between required performance and cost.

3. Converter Efficiency & Heat Management

Efficiency is an important factor that must be considered in the design of the AUV charging circuit. This section will examine all the significant sources of loss in the system based on the selected components and estimate the expect impact these losses have on overall efficiency. The loss components on interest are the power transistor, the power diode, and the output and input filter inductors.

3.1. Power Transistor Losses

The power MOSFET is the single greatest source of losses in the buck converter. MOSFET losses are the result of both switching losses (from the turning on and off of the device every duty cycle) and from I^2R conduction losses (from the passing of current through the device while on).

MOSFET conduction losses $\left(P_{FET,cond}\right)$ are:

$$P_{FET,cond} = I_{out,max}^2 \, R_{DS,on} \, D_{max} = 12.62A^2 * 0.18\Omega * 0.75 \cong 21.50W$$

MOSFET switching losses $\left(P_{FET,sw}\right)$ are:

$$P_{FET,sw} = \frac{1}{2}\left(t_{fall} + t_{rise}\right) I_{out,max} V_{in,max} f_{sw} = \frac{1}{2}(22ns + 35ns)(12.62A)(75V)600kHz = 16.19W$$

MOSFET total power losses are:

$$P_{FET,tot} \cong 37.7W$$

The chosen IRL520NPBF is capable of withstanding 48W of dissipated power, so the device is acceptable for this application. The real issue with power losses, especially in the case of the MOSFET, is that the power lost is dissipated as heat into the device and the surrounding area. This heat needs to be removed from the system through the use of appropriate heatsinks. Heatsink requirements and selection will be discussed in

3.2. Power Diode Losses

Diode power losses typically result from three loss mechanisms: conduction, capacitive charging, and reverse recovery. The Vishay Dale V12P10 is a Schottky diode. These diodes are majority carrier devices and do not have reverse recovery losses, so only calculations for conductive and capacitive charging losses are presented.

Diode conductive losses $\left(P_{diode,cond}\right)$ are:

$$P_{diode,cond} = I_{out,max} * V_f * (1 - D_{min}) = \ 12.62\text{A} * 0.58\text{V} * (1 - 0.6) \cong 2.92W$$

The capacitive charging losses are a little more difficult to calculate, because some estimation of the junction capacitance must be done to actually solve for the losses. The typical junction capacitance of the V1210 for a given reverse voltage is provided by the manufacturer and graphed in Figure 17 [22].

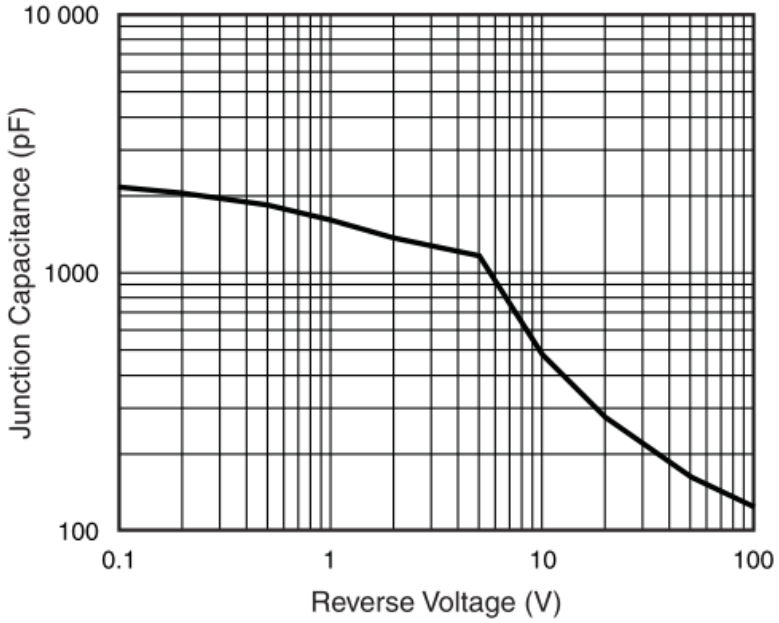

Figure 17: V12P10 Junction Capacitance vs. Reverse Voltage

The capacitive charging loss $(P_{diode,cc})$ is calculated as follow:

$$P_{diode,cc} = \int_0^Q V dq * f_{sw} \cong$$

$$[1000pF(5V - 0V) + 400pF(10V - 5V) + 200pF(40 - 10) + 20pF(75 - 60)] * 600kHz$$

$$P_{diode,cc} \cong 0.008W$$

Diode total power losses are:

$$P_{diode,tot} = P_{diode,cond} + P_{diode,cc} + P_{diode,rr} \cong 2.93W$$

3.3. Output Inductor Losses

The output inductor is another source of losses in the system. These losses are due to AC and DC I^2R losses in the copper wire and to core losses resulting from the time-varying magnetic. Estimation of these loss mechanisms was accomplishing using an online calculation provided by the manufacturer of the selected inductor.

The inductor used for this application was the Vishay Dale IHLP-6767GZ-11 15 µH surface mount inductor. It offered a high saturation current with acceptable total losses of 3.1W. The details of the loss calculator are provided in Figure 18. Core losses are greater than the recommended 1/3 total power loss, as a result of using a high switching frequency of 600 kHz. The calculator displays the warning in its Warning Message window. The 1.116W associated with core losses, however, is only slightly more than 1/3 and acceptable for this design.

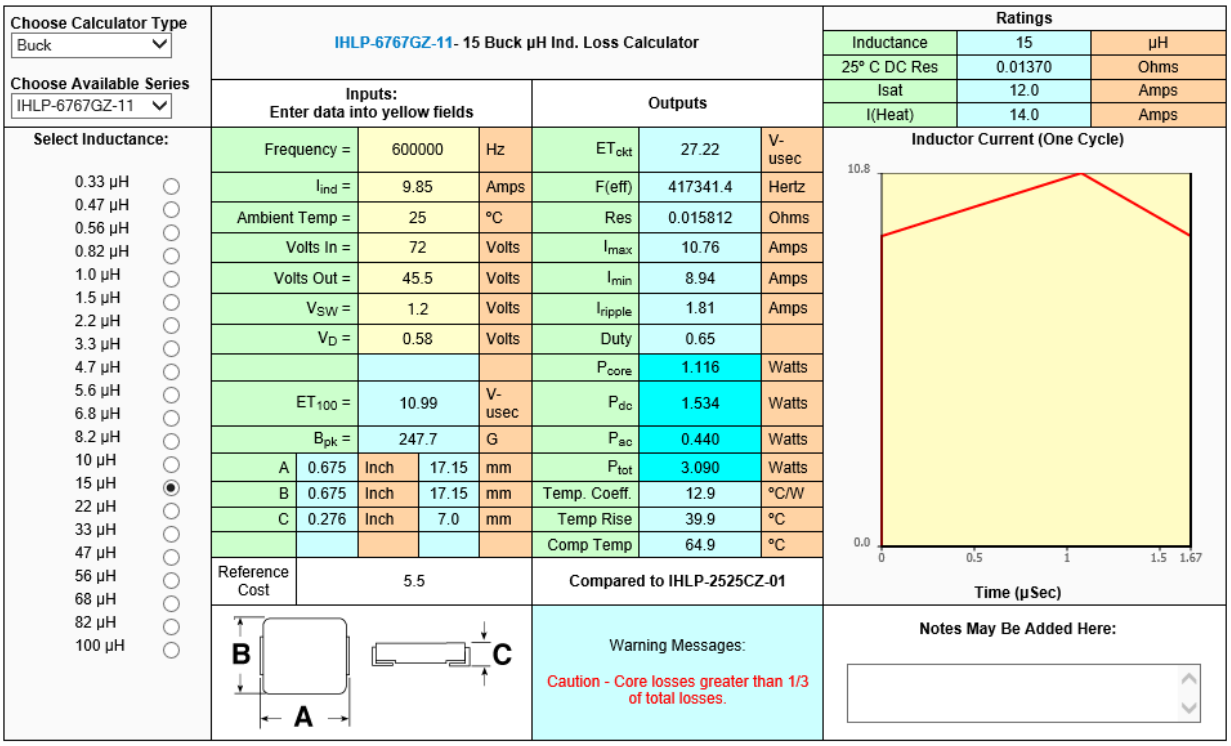

Figure 18: Inductor Power Loss Calculator provided by Vishay

3.4. Input Inductor Losses

The input inductor is the 1.0µH Vishay Dale IHLP3232DZER1R0M11. It represents little to no loss in the system even at 120Hz, but again the losses can be calculated. First, we look at I^2R losses in the core.

DC I^2R Losses $\left(P_{in}^{DC}\right)$ are:

$$P_{in}^{DC} = (i_{in,fund}^{pk-pk})^2 * R_{in}^{DC} = (7.1A)^2 * 0.00433\Omega = 0.22\ \text{W}$$

AC I^2R Losses $\left(P_{in}^{AC}\right)$ are:

$$P_{in}^{AC} = (i_{in}^{AC})^2 * R_{in}^{DC} = (4A)^2 * 0.00433\Omega = 0.07\ \text{W}$$

Core Losses (P_{in}^{core}) are:

$$P_{in}^{Core} \cong 0.01\ W$$

A more accurate calculation of core losses can be obtained using Steinmetz Equation for ferromagnetic materials. However, the ripple current on the input inductor is on the order of 10mA over the switching period, with a 4.5A ripple resulting from the full bridge rectification. The small change in inductor current over the switching period indicates negligible core losses due to negligible variations in the magnetic field. The 4.5A ripple resulting from the full bridge rectifier and smoothing capacitors have a larger impact on losses. The change, however, is over a much longer period of time at a frequency of 120Hz, again decreasing its impact on overall losses. Input inductor core losses will not be 0W, but the will be small relative to both the DC and AC I^2R losses of the inductor.

Total Input Inductor Losses $\left(P_{in}^{tot}\right)$ are:

$$P_{in}^{tot} = P_{in}^{DC} + P_{in}^{AC} + P_{in}^{core} \cong 0.3\,W$$

3.5. Overall System Efficiency

Total system efficiency under the worst case scenario can be estimated as:

$$\eta = \frac{P_{out,max}}{P_{in} + P_{MOSFET} + P_D + P_{L,in} + P_{L,out} + P_R} = \frac{500}{500 + 37.7 + 2.9 + 0.3 + 3.1 + (0.1 * 10)} = 0.92$$

The efficiency calculation presented includes power loss across the sense resistor, which has been ignored up until this point. In series with the battery pack is a 0.1Ω 5W 5% precision sense resistor. The resistor dissipates 1W of power on average. The sense resistor is included in the design to provide a voltage reference signal to the feedback system for active duty cycle adjustment during the charge cycle operation. Feedback allows for more precise determination and control of the average current being delivered to the battery pack.

3.6. Heat Management

Power losses are dissipated as heat to the device packages and the environment. With the power loss calculations presented, the worst case heat loads are:

$$P_{diode,tot} \cong 2.9W$$

$$P_{FET,tot} \cong 37.7W$$

The 3.09W heat load on output filter inductor is ignored in this analysis, because the temperature rise is this component is already known from Figure 18. The temperature rise is expected to be about 40°C; the components remains well within its acceptable temperature operating range. The 0.3W heat load on the input filter and the 1W load on the sense resistor are also ignored; these devices is not expected to be adversely affected by this relatively small heat loading.

The heat loads on the diode and MOSFET, however, need to be removed from the system either passively or with the assistance of heatsinks to ensure proper system performance and to prevent component damage and failure.

Design specifications require that each device junction temperature remain below the maximum allowable junction temperature. The maximum junction temperature for the IRL520NPBF MOSFET is 175°C and 150°C for the V12P10 Schottky diode.

3.6.1. Diode Heatsink Requirement

The maximum allowable diode junction temperature $T_{j,max}^{diode}$ is 150°C. If we then use the thermal resistivity model to calculate heat dissipation, we can determine if a heatsink is required or not.

$$T_j^{diode} = P\left(\frac{\left(R_{\theta JA} * \left(R_{\theta JL} + R_{L-PCB}\right)\right)}{\left(R_{\theta JA} + R_{\theta JL} + R_{L-PCB}\right)}\right) + T_{AMB}$$

All unknowns are provided on the datasheet with the exception of the thermal resistance of the Lead–to–PCB. Without taking actual measurement on the final board, an estimate is required. Vishay semiconductors recommended following some good design practices, such as being generous with the pads and ensuring good solder connections. These practices were followed. The rule of thumb for temperature estimate was given as $40\frac{^\circ C}{W}$. Using this estimate, we have:

$$T_{j,max}^{diode} = 2.9W\left(40\frac{^\circ C}{W}\right) + 25^\circ C$$

$$T_j^{diode} = 141^\circ C$$

This is a worst case estimate, meaning the Vishay V12P10 Schottky rectifier should be a acceptable choice for this application. The above calculations shows that the junction temperature of the device will remain well below the thermal limit of 150°C, and a heatsink is not required. This temperature should be checked during testing to ensure the temperatures does in fact stay below the required threshold. This can be done with a laser temperature probe or other appropriate measuring device.

3.6.2. MOSFET Heatsink Requirement

The IRL520NPbF MOSFET has a maximum allowable junction temperature $T_{j,max}^{FET}$ of 175°C. Because the power dissipation is expected to be 37.7W, a heatsink will absolutely be required. Below we calculate the maximum thermal resistance using the rule of thumb formula recommended by International Rectifier.

$$R_{\theta HS,FET} \leq \frac{(T_{SINK} - T_{AMB})}{P_{FET,tot}}$$

$$R_{\theta HS,FET} \leq \frac{(90^\circ C - 25^\circ C)}{37.7W}$$

$$R_{\theta HS,FET} \leq 1.72\frac{^\circ C}{W}$$

The IRL520NPbF comes in a TO-220 package. A standard natural convection heatsinks for this particular package cannot provide the required thermal resistance levels. The lowest thermal resistance for TO-220 packages readily available from multiple vendors like Digikey and Aavid Thermalloy is approximately 2.6 °C/W. As an example, the Aavid Thermalloy 530002B00000G extruded heatsink with large radial fins is provided in Figure 19. This product would be ideal if it had a lower thermal resistivity.

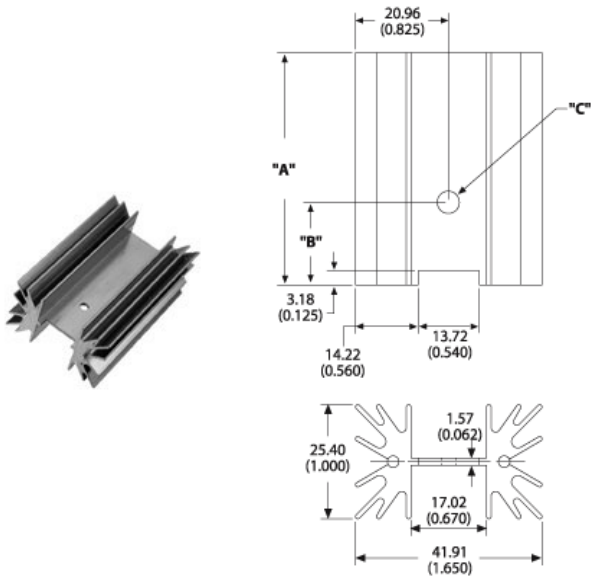

Figure 19: Aavid Thermalloy TO-220 Heatsink

A custom heatsink is required. One particular solution for prototyping is a custom 64315 2" heatsink from Aavid Thermalloy (Figure 20). The heatsink is quite large at 5.5" in width and 2.0" in height. However, with a length of 2", an acceptable thermal resistance of something less than 1.53°C/W can be reached.

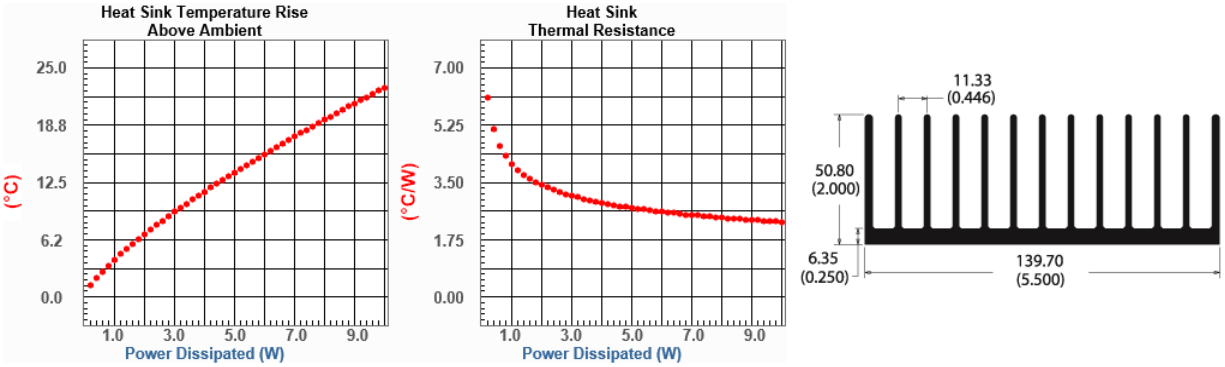

Figure 20: Aavid Thermalloy 64315 Heatsink

There is, of course, and alternative approach as well. A MOSFET with lower power losses can be identified and incorporated into the design. Power losses can be minimized by finding a MOSFET with a lower on resistance, a lower junction-to-case thermal resistance, and faster rise and fall times. The objective is always to minimize losses to increase efficiency. The IRL520NPbF was chosen because it was a good engineering fit for the project. A better device might be available. This is an area for future evaluation and refinement.

A final note about heatsinks is required, because of the environment in which this converter is intended to operate: the pressure housing of the AUV. The ocean is generally speaking very cold with temperature ranging from 2°C to about 32°C maximum. The AUV will most likely spend most of its time in less than 10°C waters and approach the surface to recharge in waters in the 20°C range. There is an excellent opportunity to use the environment to dissipate heat emanating from charging by using the

AUV housing as a heatsink. Mounting the converters to the AUV shell while electrically insulating the components from shorting would allow heat to be dissipated from the shell to the cold water surrounding the vessel. In this case, forced convention might not be required at all, because adequate surface area and cooling flow would be available to operate the converters indefinitely without concern for heat damage. Again, the precise method of incorporating this design into the AUV will require some additional development work and research. The important point is that heat will be generated, and it will need to be dealt with appropriately to prevent charging system damage and potential battery pack malfunction.

4. Feedback Design

The decision to include active duty cycle control through the use of negative feedback was driven by the need to precisely regulate the output current to within a very small window of variation to prevent damage to the battery pack. Because the battery pack represents an effective series resistance (ESR) on the order of milliohms (mΩ), a relatively minor change in output voltage has the potential to greatly increase or decrease the output current. The objective of feedback is to self-correct for these conditions in such a way that the battery pack a) builds to 10A without overshoot when charging is initiated, and b) never experiences a transient current response greater than 14A, as specified by the design requirements of Table 1. These requirements are competing. The desire to not overshoot suggests a slow controller while the desire to response quickly to transients suggests a fast controller. An appropriate feedback design was needed to regulate the output current under all operating conditions. Two approaches to feedback were explored.

4.1. Hysteretic Control

The first attempt at feedback control was with the use of hysteretic control. Hysteretic control is an interesting concept and has been used quite effectively in other power applications. Figure 21 shows an overview of the nominal hysteretic controller.

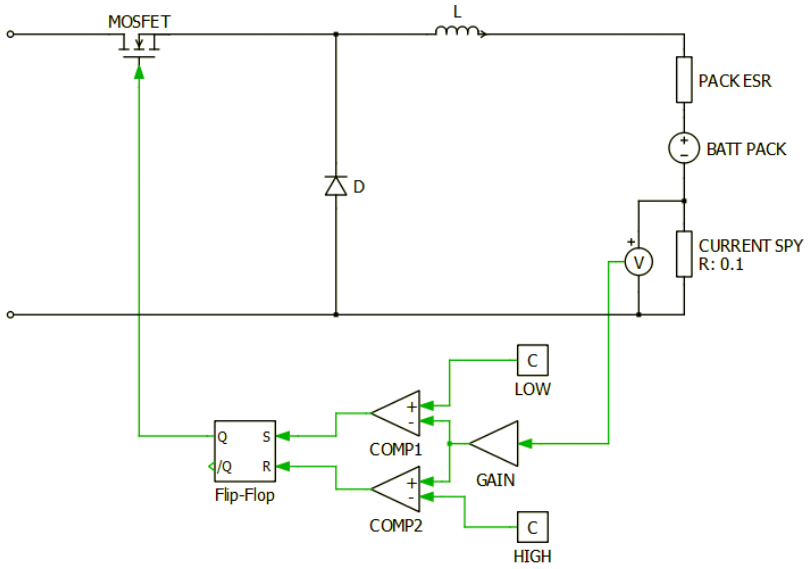

Figure 21: Hysteretic Controller for Buck Converter

The hysteretic controller functions by continuously sensing a voltage and comparing that voltage to two threshold voltages: a high threshold and a low threshold. The comparison is accomplished with the use of two comparators. The two outputs of the comparators are then input into an appropriate flip-flop. The flip-flop's output is then used to provide the control signal to the MOSFET's gate.

Conceptually, the idea is great. By constantly comparing the sensed voltage to thresholds, the designer can ensure both controller speed and stability. In practice, however, the hysteretic controller can be quite difficult to realize. Preliminary efforts to build this control involved converting the sensed voltage to a digital value using an analog-to-digital converter (ADC). The digital signal was then compared in software to generator the output signal. It was much harder to guarantee a baseline switching

frequency of 600kHz with this approach. Also, it was much harder to ensure that enough samples were being taken to ensure proper system performance. A Cypress Semiconductors PSOC5LP Development Kit was used for this project. The onboard ADC and flip-flops proved too slow to effectively implement this controller at 600kHz. A lower switching frequency might have worked better, but the resolution required to properly modulate the duty cycle simply was not available with the chosen microcontroller system.

4.2. Proportional – Integral – Derivative (PID) Controller

Another option for feedback was the Proportional, Integral, Derivative (PID) controller. The PID controller is an industry standard. It takes an error signal and performs three separate calculations, sums the results, and provides the result back to the input of the system. The three calculations performed are a proportion gain, an integral gain, and a derivative gain, as suggested by the controller's name.

For the purposes of the feedback analyze, only the small signal model of the buck converter is considered. This simplification removes the input filter from the transfer function *H(s)*. The small signal averaged model of the buck converter produces the following state equations:

$$\frac{d\bar{i_L}}{dt} = \frac{\overline{v_{in}}*d}{L} - \frac{\overline{v_o}}{L} \qquad \& \qquad \frac{d\overline{v_c}}{dt} = \frac{d\overline{v_o}}{dt} = \frac{\bar{i_L}}{C} - \frac{\overline{v_o}}{RC}$$

These state equations are linearized about the operating points $\overline{v_o}$ and d. The input voltage $\overline{v_{in}}$ is assumed to remain relatively constant during operation. *H(s)* then becomes:

$$H(s) = \frac{\widetilde{v_o}(s)}{\tilde{d}(s)} = \frac{V_{in}}{LC}\left[\frac{1}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}\right]$$

H(s) has 2 left-hand poles (LHP) with no zeroes, as seen by the denominator. Matlab® was used to solve numerically for *H(s)*. With V_{in}= 72V, R = 0.072Ω, L = 15µH, and C = 130µF:

$$H(s) = \frac{4.8e6\ s + 5.13e11}{s^2 + 1.07e5\ s + 5.13e8}$$

The standard model for closed loop feedback is shown in Figure 22.

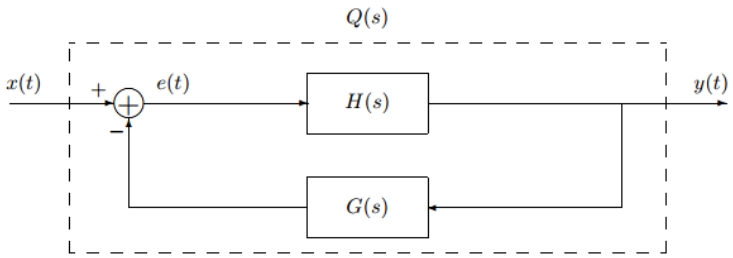

Figure 22: Standard Closed Loop Feedback Model

H(s) is known. *G(s)* must be found. *G(s)* for a PID controller is, as previously mentioned, the summation of a proportion gain, an integral gain, and a derivative gain. Figure 23 illustrates the PID Controller.

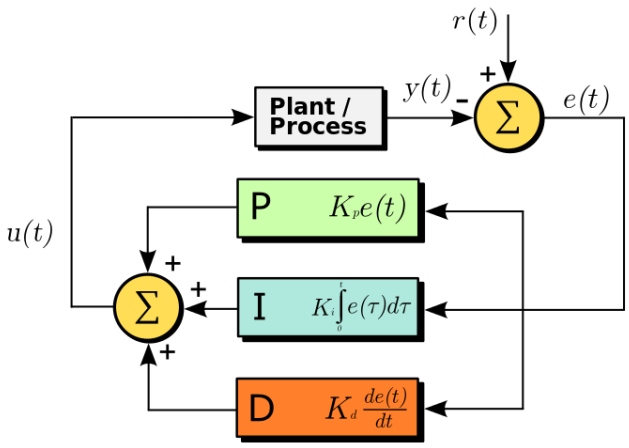

Figure 23: PID Controller Block Diagram [23]

The error signal *e(t)* shown in Figure 23 is generated by comparing the sensed voltage to the desired voltage. Again, an ADC is used. The error signal then simply becomes the difference between desired voltage of 1V and the sensed voltage. The gain factors K_p, K_i, and K_d remain unknown. There are several way to determine what the individual gains of a PID controller ought to be. The process of identifying these gains and producing the controller response is called tuning.

The Matlab® function "pidtool" is great for tuning a PID controller. This function was used in conjunction with Simulink® to define *G(s)* and model the resulting controller performance. The process was iterative. There is not a unique solution to *G(s)* using this method. The gains can be varied as the designer sees fit to produce the required system response. The design goal for this application was to achieve a balance between controller response speed and the desire to reduce system overshoot resulting from the initiation of the charging evolution. The gains were varied using "pidtool" to produce an acceptable response. The response was evaluated in Simulink® using a simplified circuit model and then again validated with PLECS® using a complete circuit model.

Several useful output are produced during the tuning process, including the step response and bode plots of the controller. Figure 24 shows the step response of the selected PID controller. The response amplitude is allow the peak at nearly 140% of the desired output amplitude with the selected controller. The simulation data will show that this response characteristics is the maximum controller overshoot that allows the output to approach the 10A without overshooting it during charge initiation. The controller output settles within approximately 1ms, and the controller is always stable.

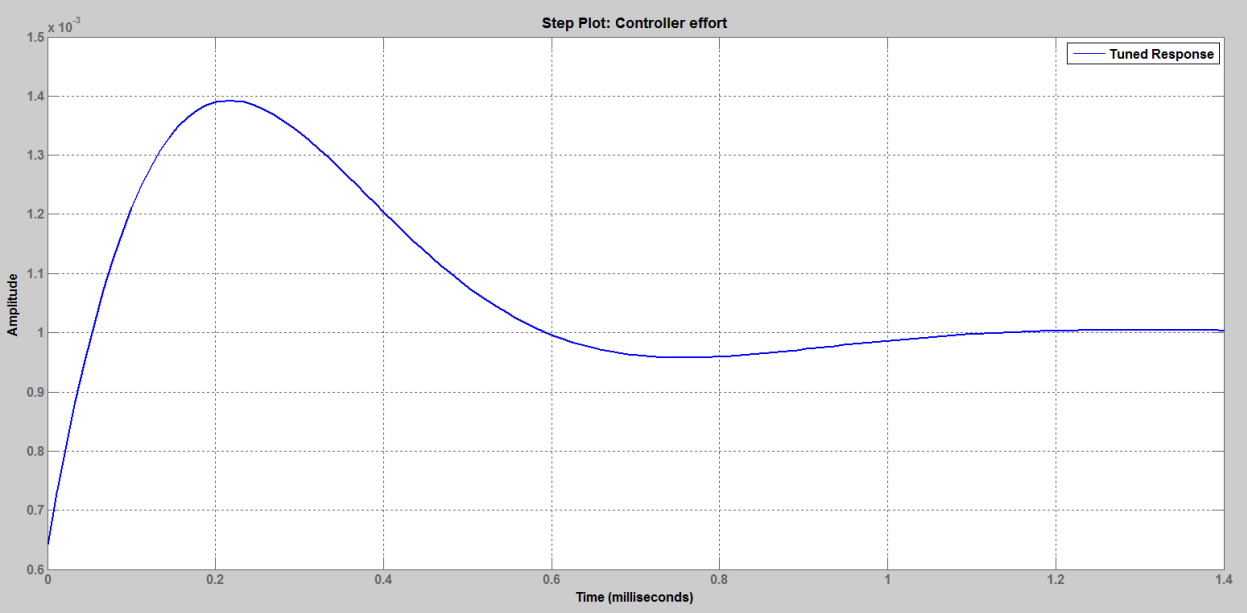

Figure 24: Step Response of Selected PID Controller

Figure 25 shows the bode plot of the selected controller. Both the magnitude and phase of the response is plotted. The peak response occurs at the corner frequency 6.57kHz – well below the switching frequency for the MOSFET. Also note that the response is always attenuated.

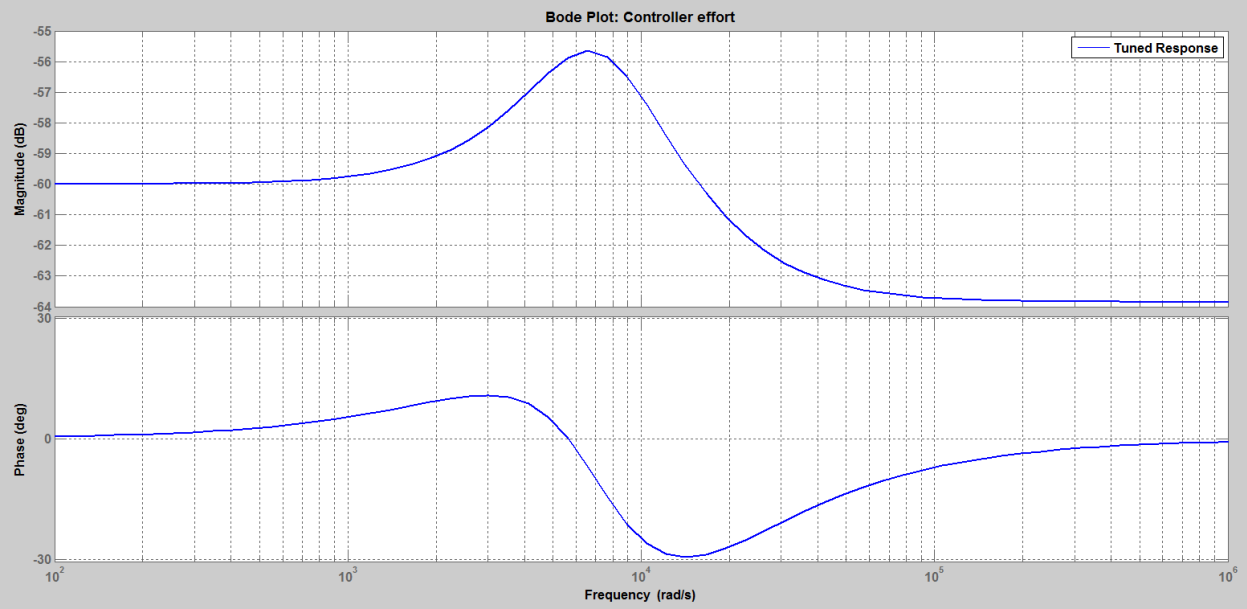

Figure 25: Bode Plot of Selected PID Controller

The most important output of the "pidtool" are the controller gain factors K_p, K_i, and K_d. The controller gains were:

$$K_p = 0.00064 \cong 0 \qquad K_i = 10.0606 \qquad K_d = 0$$

4.3. Simulink® Modeling Validation of Selected Integral (I) Controller

The results of the Matlab® "pidtool" suggest that the controller should be an Integral (I) Controller. To validate the response of the system, a Simulink model was developed. The model is cursory as it only looks at the output of the buck controller and assumes the input is a stable 72VDC. A complete model was built and tested using PLECS. The results of the PLECS model will be presented later.

Figure 26 illustrates the Simulink® model that was used for controller validation. Again, the input voltage V_{in} is a fixed DC voltage. The gains of the PID controller are incorporated into the model in the C1 LTI System block. A saturation limit of 85% is included to prevent the duty cycle from reaching 100%. The saturation limit ensures the system will always operate as a pulse-width modulator (PWM), properly cycling the MOSFET each switching period.

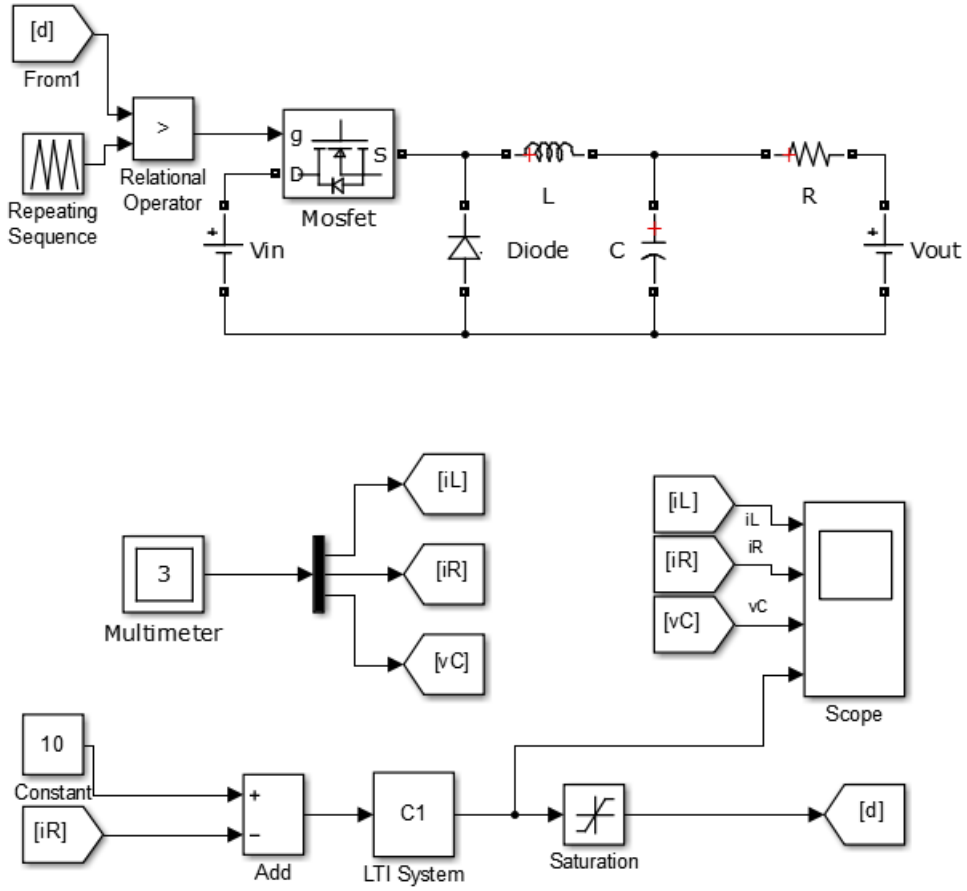

Figure 26: Simulink® I Controller Model

The Simulink® model contains a scope with four inputs, as seen in Figure 26. The first input is the current through the output inductor (iL). The second is the current through the sense resistor (iR). The output capacitor voltage (vC) and the duty cycle signal (d) are also probed. The goal of the simulation is to confirm that the controller does in fact produce a regulated 10A of current through the sense resistor R without overshooting. The three additional signals on the scope provide insight as to how the system is operating as a whole. Most importantly, iL should show the transition point from discontinuous conduction mode (DCM) to continuous conduction mode (CCM) as current through the induction L

builds. The system was designed to operate in CCM in steady-state, so the simulation should validate this operational feature as well.

A 20ms simulation was run in Simulink® with the model from Figure 26. The results of the simulation are provided in Figure 27. From the plots the first point to notice is that 10A is approached gradually with no overshoot. 10A is reached within the first 7ms of operation. The plot of the current through the inductor (iL) also shows the transition from DCM to CCM quite clearly. At approximately 6.5ms, the current builds up enough to enter CCM.

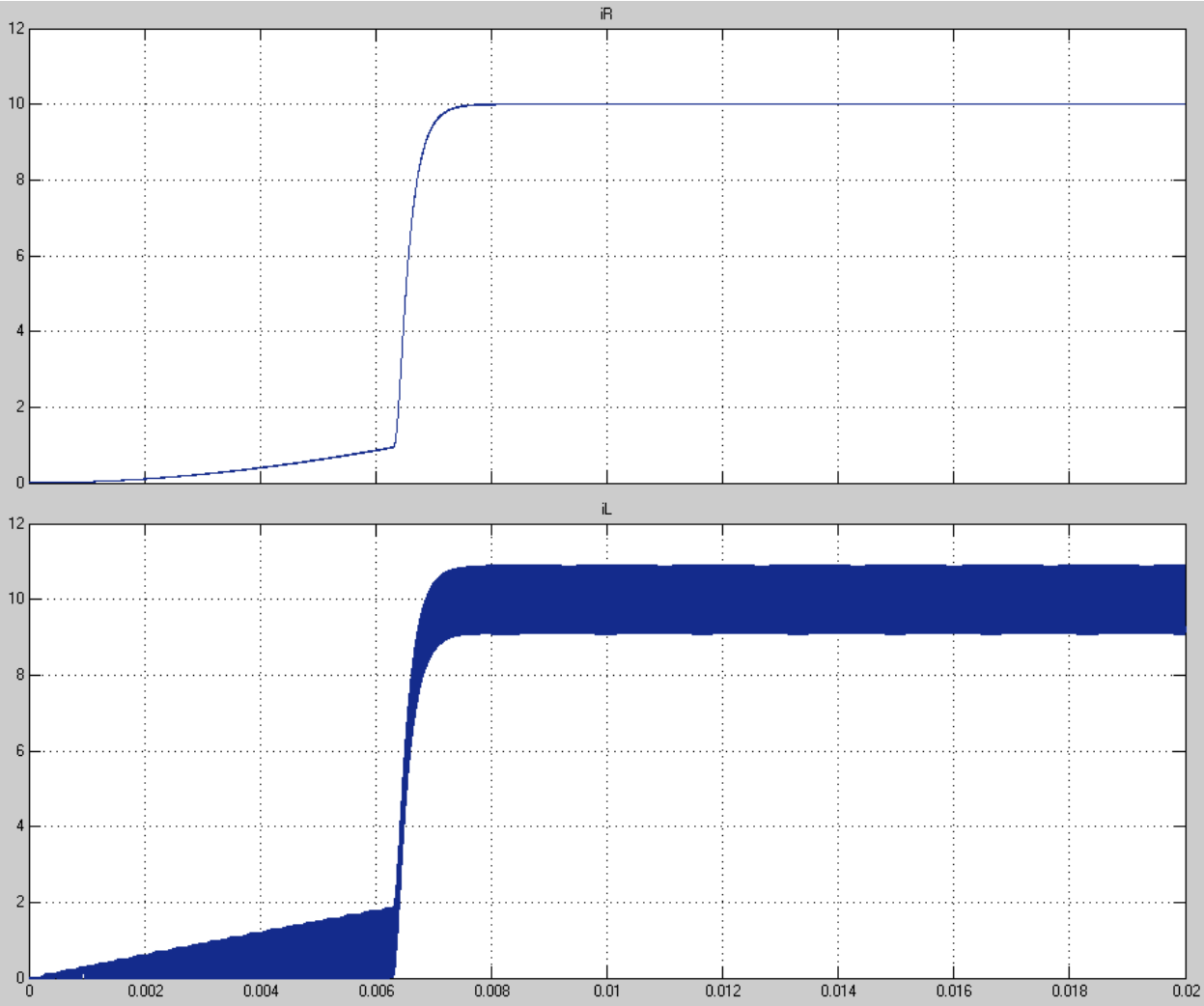

Figure 27: Simulink® Output of Sense Resistor Current (iR) & Inductor Current (iL) with I Controller

The Simulink® results validate the controller's performance. A faster response was possible with a larger K_i, but not without potential overshoot. A gradual build to 10A is much preferred to potentially damaging the battery pack during the initiation of charging. The current ripple on the output inductor is also important to note. It looks to be on the order of 2A from the plot. This result confirms the calculation presented in 2.7 and the result provided in the power loss calculator of Figure 18.

Implementation of the controller was achieved with the use of a Cypress Semiconductors PSOC® 5LP Development Kit. The PSOC 5LP is a very capable programmable system-on-a-chip with numerous analog and digital input and output components.

To realize the PID controller, the current sense voltage signal was input into an onboard ADC. The digital voltage was then converted to a current and compared to the desired current. An error signal result, which was then multiplied by $K_i = 10.06$, as shown. The error signal was then used to adjust the duty cycle of a 600kHz built-in digital Pulse Width Modulator (PWM). The duty cycle initiates are 10%, and builds to the required level in response to the error signal. Error calculations and duty cycle updates occurred in lab testing at an approximate frequency of 12kHz with this approach. Testing also showed the current regulation to be quite precise over a range of currents. Testing was conducted to regulate current at 1A through the rate 10A was consistent, acceptable current regulation. More testing is required to validate the robustness and reliability of this approach, but initial testing was promising.

The PSOC code used for this application is available upon request and is adaptable for any required PID controller solution.

5. MOSFET Driver Design

Designing an appropriate driver for the MOSFET gate signal represented a significant challenge to the overall circuit design. The challenge stemmed from the easily overlooked physical location of the MOSFET in the buck converter (Figure 11). The source of the device is not referenced to the ground potential; it is floating. Since it is the voltage potential between the source and the gate (V_{GS}) that determines the ON state of the device, a MOSFET driver that could generated the required V_{GS} to switch the device at the design switching frequency was needed.

5.1. IR2125PBF MOSFET Driver

The IR2125PBF Current Limiting Single Channel Driver was selected to drive the MOSFET gate signal. The device features a floating channel designed for bootstrap operations up to +500V with a typical on/off time of 150ns [24]. The device can also be run off input logic down to 2.5V.

What makes this particular integrate circuit (IC) attractive for this application is the fact that it is designed specifically to drive floating channel MOSFETs. It does this with the use of a bootstrap capacitor that is connected between the supply rail and the MOSFET source voltage (V_s). Figure 28 shows the typical wiring of the IR2125PBF [24]. For this application, the current sensing feature of the IC is not used. As a consequence, the CS pin is hardwired to V_s directly.

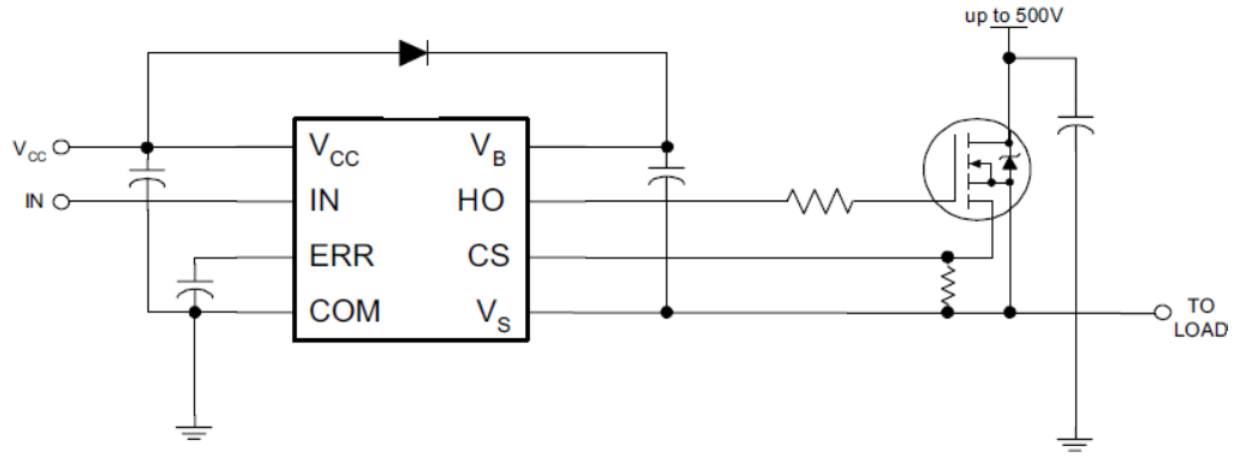

Figure 28: Typical Connection of IR2125PBF Driver to MOSFET Gate

The datasheet provided the typical connections for the IR2125PBF. The application notes provided guideline for properly sizing the various capacitors and resisters needed to successfully operate the device [25]. The final design with all components sized and connected is shown in Figure 29. Both electrolytic and metal film capacitors were used to provide the required input capacitance. A 220µF electrolytic bulk capacitor was used between V_{cc} (Pin 1) and Gnd (Pin 4). In parallel with this capacitor was a 0.82µF metal film capacitor. These capacitors together serve to provide a stable input voltage rail for the IC. Another 0.015µF metal film capacitor was used between ERR (Pin 3) and Gnd (Pin 4), as required by the application note [25].

The bulk bootstrap capacitor between V_B and V_S was chosen to be another 0. 82µF metal film capacitor. Metal film was used exclusively for the bulk capacitor because of its excellence performance during high frequency operations. The final component selected for the drive circuit was the charging diode

between V_{CC} (Pin 1) and V_B (Pin 8). A MUR120 was used because it is rated to up to 1A average current and a peak repetitive reverse voltage of 200V [26]. A 10Ω ¼W resistor was also placed in series with the output pin (H_o) as suggested by the application note to reduce inductive ringing in the control signal.

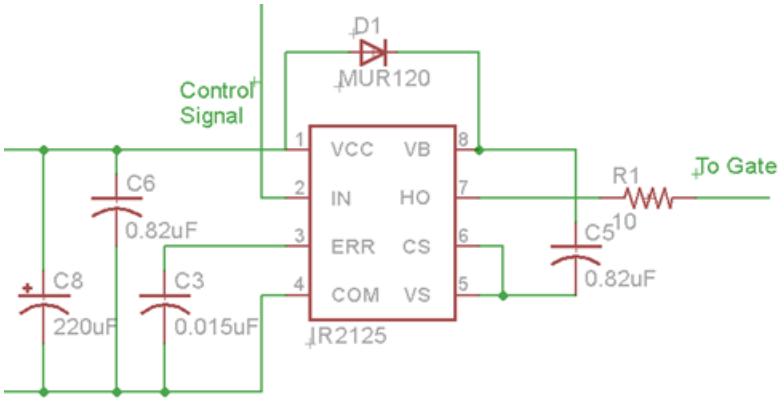

Figure 29: Final Design of Driver Circuit

5.2. Driver Power Supply

The IR2125PBF does require a DC input voltage V_{cc} for operation. The maximum V_{cc} can be is 25V. For simplicity, 15VDC was chosen as the design voltage for V_{cc}. 15V ensures the IC receives sufficient voltage to operate properly under all conditions. Also, since V_{cc} determines the voltage delta above V_s achieved by the driver, 15V also ensure that V_{GS} will drive the MOSFET hard ONMOSFETs that are soft ON tend to generate much high I^2R losses than those that are hard ON, so it is very desirable from an efficiency and heat management perspective to ensure the device is always driven hard ON.

15VDC, however, is not available in the circuit. It needs to be generated. The solution proposed for generating 15V was to use a bipolar-junction transistor (BJT) Zener diode voltage regulating circuit, shown in Figure 30. The circuit uses a Zener diode to hold a constant voltage on the base of a BJT.

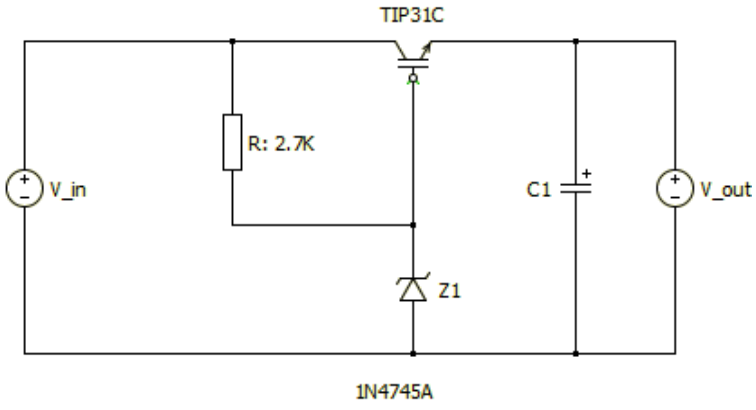

Figure 30: BJT-Zener Diode Voltage Regulating Circuit

The input voltage V_{in} originates from the rectified voltage output of the full-bridge rectifier and smoothing capacitors. V_{in} is approximately 70VDC. The current drawn by the Zener diode is limited by

the resistor R. In this case, the Zener diode Z1 was selected to be the 16V 1N4745A. At 16V, Z1 requires an average current of 15.5mA and a maximum current of 17mA.

To ensure that Z1 would be driven on, the limiting resistor R was selected to be 2.7kΩ. V_{in} will be the rectified and filtered input voltage to the MOSFET and will range from 60-75VDC. Therefore, the voltage on the base of the BJT is guaranteed to be 16VDC at all time. V_{out} can now be calculated as:

$$V_{out} = V_B - V_{BE} = 16V - 0.6V = 15.4V$$

The BJT-Zener diode voltage regulating circuit will supply the stable rail required for the proper operation of the MOSFET IR2125PBF driver IC. The only unresolved issue is the circuit's effect on power. Power is dissipated in the resistor R, the Zener diode Z1, and the BJT. The BJT was chosen to be the Fairchild Semiconductor TIP31C. It is a 100V, 40W rated NPN BJT in a TO-220 package.

An easier solution would have been to find a 15VDC linear voltage regulator. However, the input voltage of approximately 70VDC made finding an acceptable voltage regulator difficult. Because the selected BJT is capable of dissipating 40W, there is also a certain level of robustness built into this particular solution that would otherwise not be available in an integrated IC linear voltage regulator. That say, this particular part of the circuit is an area that could be refined during future development and testing.

To calculate power dissipate, an input voltage of 70VDC and an output voltage of 15.4V is assumed.

Resistor Power: $P_R = \frac{\Delta V_R{}^2}{R} = \frac{(70V-16V)^2}{2.7k\Omega} = 1.08\ W$

BJT Power: $P_{BJT} = V_{BE}I_B + V_{CE}I_C \cong V_{CE}I_C = 54.6V * 80mA = 4.4W$

Zener Diode Power: $P_Z = V_Z I_Z = 16V * 17mA = 0.27W$

Total Regulator Power: $P_{BJT-Z} = P_R + P_{BJT} + P_Z = 1.08W + 4.4W + 0.27W = 5.75W$

The net impact of the BJT-Zener voltage regulator circuit on the buck converter is a 1% reduction in system efficiency. The system is predicted to be approximately 91% efficiency, slightly above the target of 90%.

6. Circuit Modeling & Simulation in PLECS®

Performance validation of the complete charging circuit was conducted in Plexim's PLECS®. PLECS® is a software package designed specifically for modeling and simulating dynamic systems. It is especially well-suited for power electric applications, because of its extensive built-in library of customizable electronic components. A variety of other simulation software packages, such as Cadence's PSpice®, exist and could have been used, but personal knowledge of and access to PLECS® made it the right solution for this project.

The goal of modeling was to build an accurate representation of the circuit that could later be used to assist in the printed circuit board (PCB) design effort. The goal of simulation was to validate the behavior of the circuit and to assist in component selection. For example, the ability to visually examine the voltage and current waveforms that the MOSFET was expected to encounter during operation was especially helpful in the selection of that component. The same was true for all the major components in the circuit. PLECS also allows for individual components to be updated with various characteristics once components have been selected. The forward voltage of each diode, for example, can be entered into the model once the actual diode's forward voltage is known. The ability to customize components in this manner adds fidelity to the model and greater credibility to simulation results.

Not all aspects of the circuit could be completely modeled. Limitations in the software's ability to model the control circuitry prevented individual control circuit components from being entered into the model. Instead, control blocks are used. These blocks represent the expected controller functionality, but not its physical implementation. The effect of the model's limitations on simulation results are minimal; the core of the circuit is well captured by the model. In the following section, the model and simulation results will be presented, explained, and the overall circuit design validated. Of particular interest is the final output of the charging circuit. The design goals was to create a 10A regulated current supply. The output current waveform during charge initiation, charging, and charge completion will be presented and shown to produce a well-regulated 10A current supply.

6.1. Complete Charge Circuit Model

The full model of the charging circuit consists of seven distinct sections or segments (Figure 31). In the first circuit segment, AC power is delivered to the circuit from the test source and transformed to a lower voltage. The full bridge rectifier and smoothing capacitors converter AC to DC in the second segment. The input power is then filtered through the 2nd order input filter and passed to the power switches for DC-DC power conversion. The output 2nd order filter then conditions the voltage and current waveforms in the 5th segment for delivery to the battery pack.

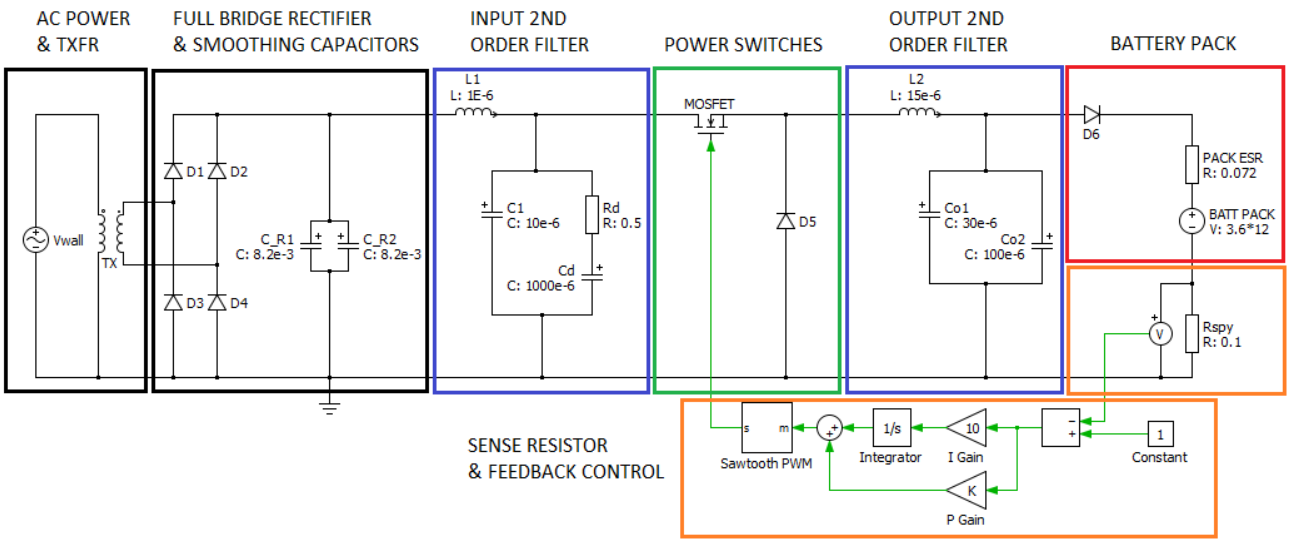

Figure 31: Full Circuit PLECS® Model with Sections Highlighted

A diode was added at the input to the battery pack to prevent the battery voltage from attempting to reverse power the converter. It serves as a one-way valve, as shown in the battery pack section of Figure 31. The sense and control circuit models appear in the block blocks. The sense resistor is accurately modeled as a resistor, while the voltage signal is approximated with the use of a voltmeter and feedback control blocks. The output of the feedback model drives the gate of the MOSFET, permitting simulation of the complete circuit. The next section will examine the voltage and current waveforms as they transit through the system to the battery pack.

6.2. Simulation Results & System Waveforms

Numerous simulation of the circuit model presented in Figure 31 were conduct during the design process. To validate the performance of the circuit, voltage and/or current waveforms were examined at the entry and exit of every stage of the system.

The first stage of the system is a 2.3:1 transformer followed by the full bridge rectifier with smooth capacitors. Because the transformer is 2.3:1, the 120VAC input is expect to be transformed to an approximately 52VAC waveform. The transformed waveform appears in the top of Figure 32.

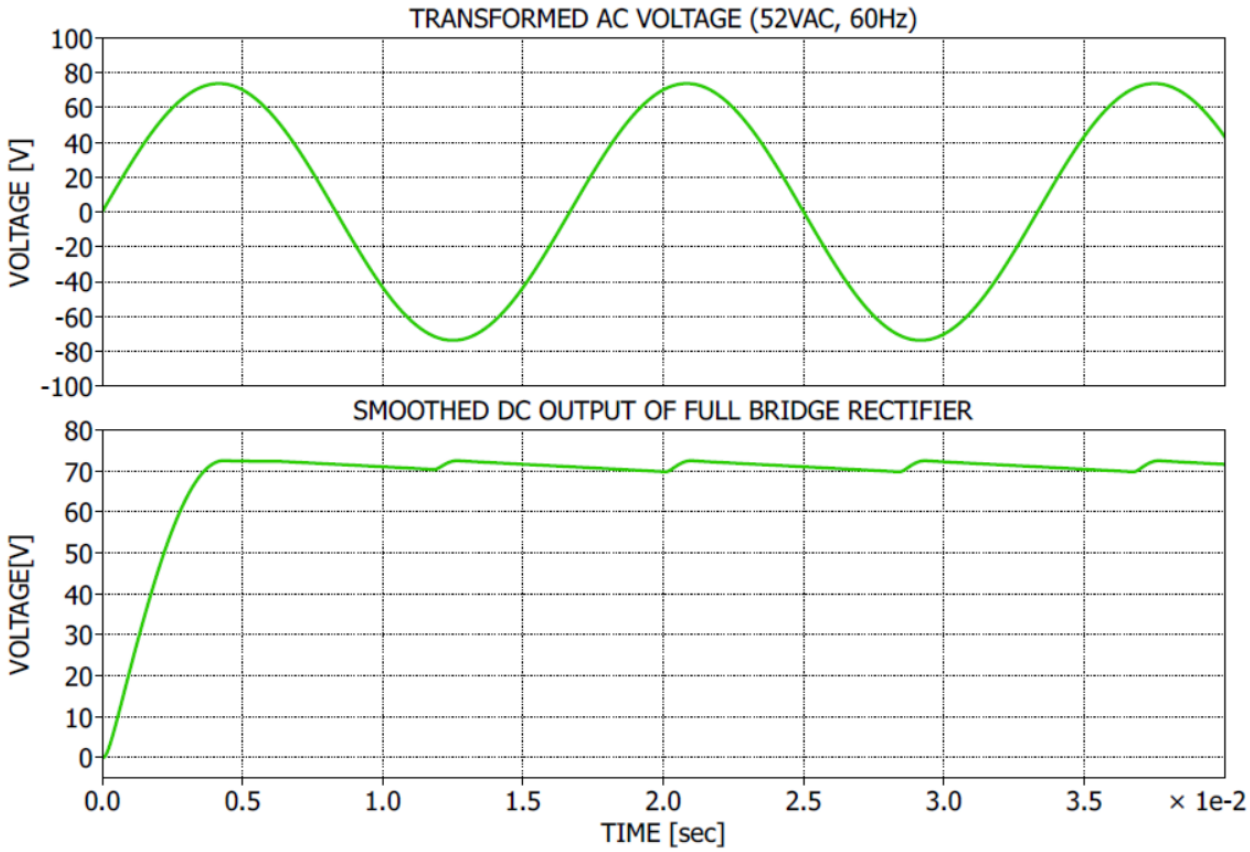

Figure 32: Transformer and Smoothed DC Output of Full Bridge Rectifier Voltage Waveforms

The transformed voltage is then rectified with the use of a full bridge rectifier. The expect peak output voltage is $52\sqrt{2}$, or 73.5VDC, minus double the forward voltage drop (V_f) of the diodes used in the full bridge rectifier. V_f is approximately 0.5V for each diode, so the expected peak voltage should be around 72.5VDC. This is clearly shown in the second waveform of Figure 32.

The addition of smoothing capacitors at the output of the full bridge rectifier permits a gradual decrease in peak voltage and holds up the voltage until the second half of the diode bridge commutes and rectifies the opposite swing of the input AC waveform. With the two waveforms of Figure 32 align in time, it is easy to see that peaks in the smoothed rectifier output coincide with positive and negative peaks in the input AC waveform.

An important feature of the charging circuit not to be overlooked is that the smoothing capacitors do not filter out the 120Hz rectified input frequency. A 120Hz ripple is riding on the approximately DC input voltage. The ripple voltage is not filtered out by the 2nd order input filter or the 2nd order output filter. Figure 33 shows that 2nd order input filter simply passes the ripple along to the power converter. A 60Hz ripple will therefore be present in the battery pack current waveform, as will be shown later in Figure 39. The 60Hz ripple is not necessarily a problem for two reason. First, the batteries can tolerate small voltage and current fluctuations to some extent as long as the average charge current is steady and stable. Second, the final design will not be using a wall outlet at 60Hz for its power supply, as previously noted. The input filter is therefore expected to complete smooth the input voltage and eliminate this problem in the final application.

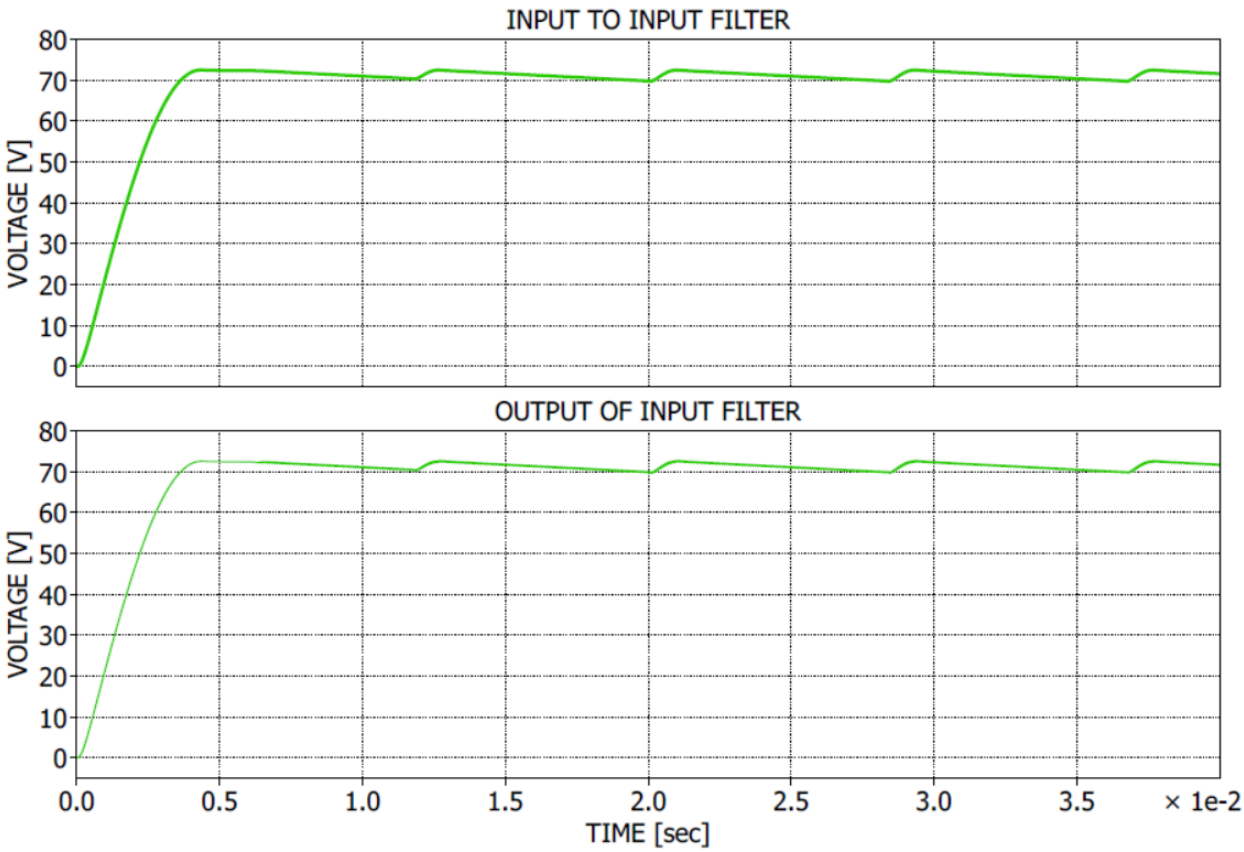

Figure 33: Input Filter Voltage Wave Forms

For comparison and validation purposes, Figure 34 is provided. The input waveform frequency was adjusted to 1MHz and the output of the input filter observed. The filter completely removes the high frequency of the input waveform and a much cleaner DC voltage is achieved at the input to the power MOSFET. The selected smoothing capacitors can and should be greatly reduced in capacitance for the final design to save volume, weight, and cost. The larger capacitors used were necessary because the 120Hz test source. With power transfer in the 1MHz range, large capacitors will no longer be necessary and should be optimized for final packaging and application.

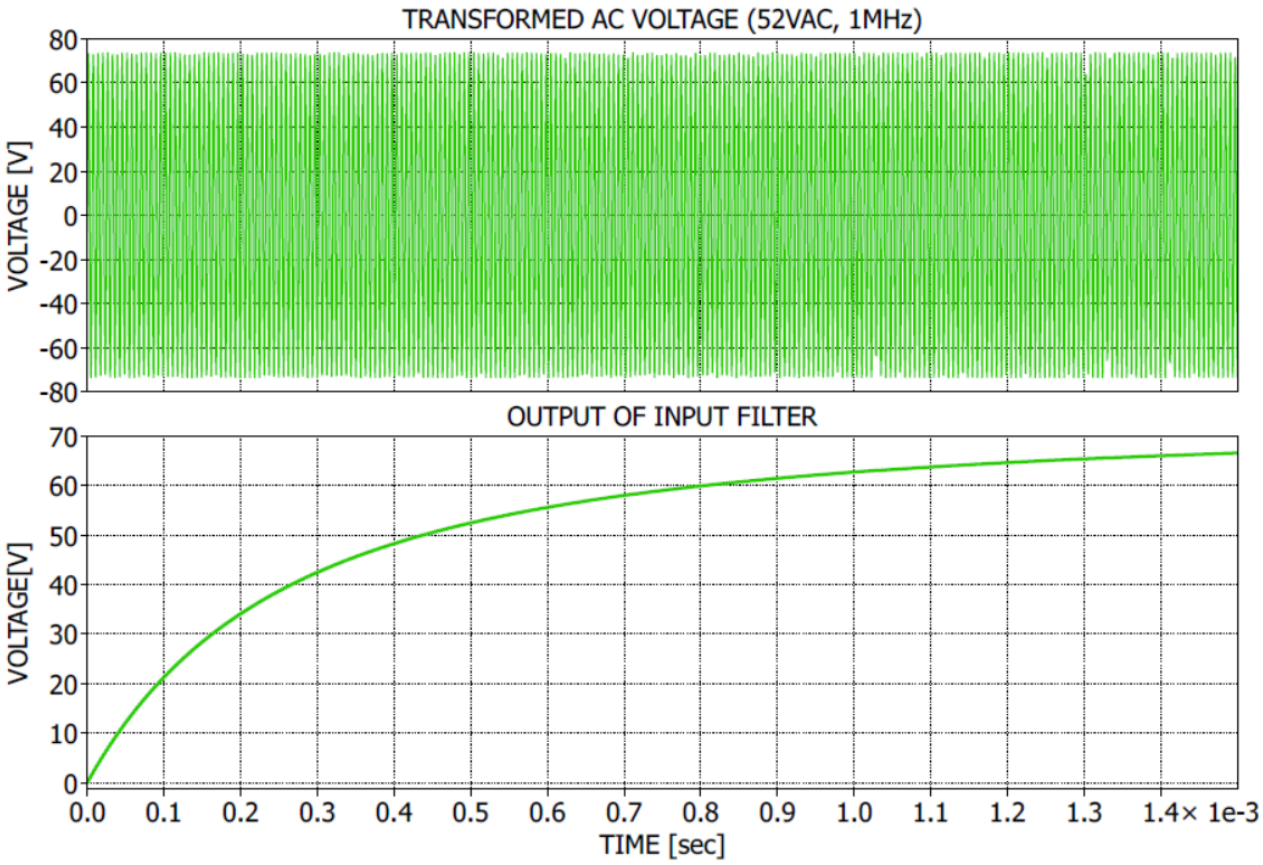

Figure 34: Output of Input Filter with 1MHz AC Input Voltage

The next set of waveform that need to be examined are the average voltage and current waveforms of the MOSFET, which are provided in Figure 35. The calculation from 2.5 indicate that the maximum average current the MOSFET is expected to encounter is approximately 7A. The MOSFET average current plot from Figure 35 can be used as a sanity check to verify this calculation. The averaging period for these plots is $\frac{1}{f_{sw}}$. This period was used to provide greater understanding of what was happening in the MOSFET over the switching period. When $\frac{1}{120Hz}$ is used for the averaging period instead, the average MOSFET current becomes a flat 6.45A during steady-state operation. This result and the bottom waveform of Figure 35 correspond with how the circuit is expected to operate. The average voltage waveform is less informative. However, it is known that input voltage is approximately 70VDC and the output voltage of the converter is approximately 45VDC. Therefore, the MOSFET should on average experience a 25VDC drop across its drain to source. The top plot of Figure 35 shows the expected steady-state voltage drop across the MOSFET after the start-up transient peak voltage.

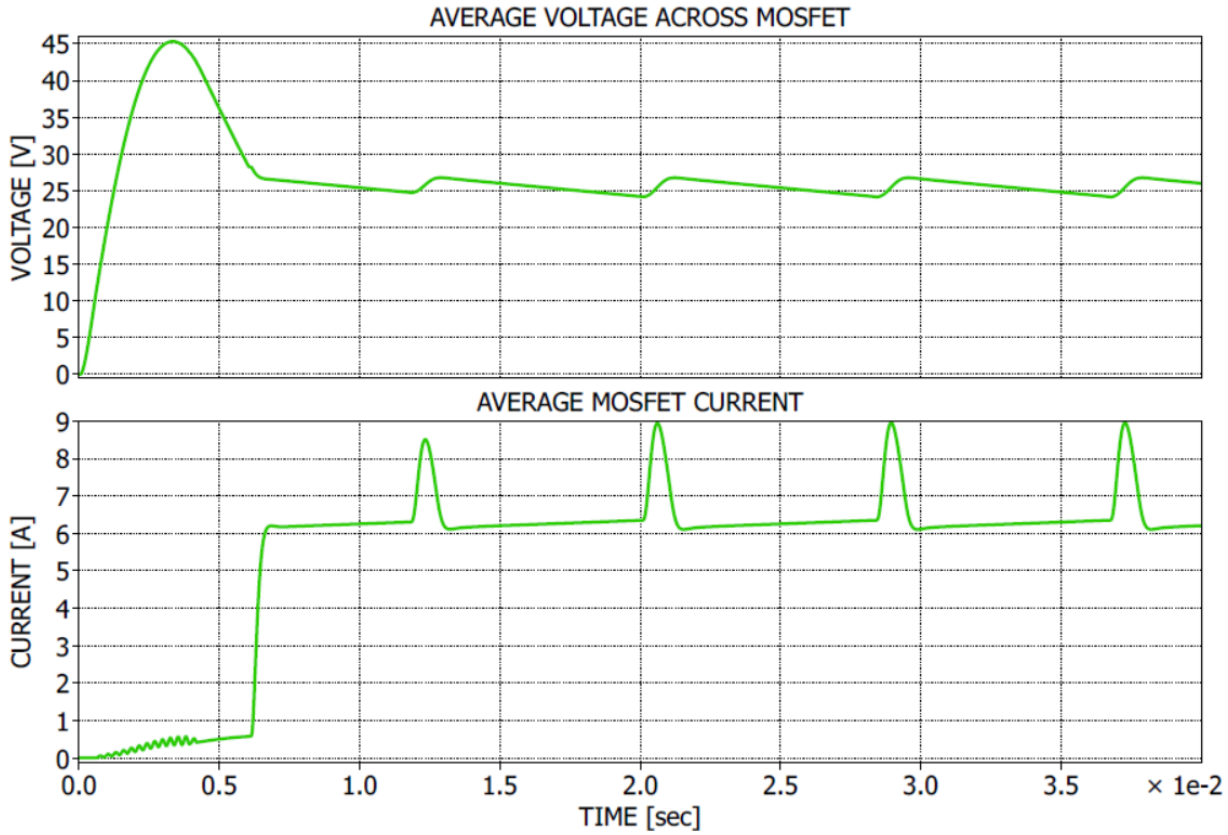

Figure 35: Average MOSFET Voltage and Current Waveforms

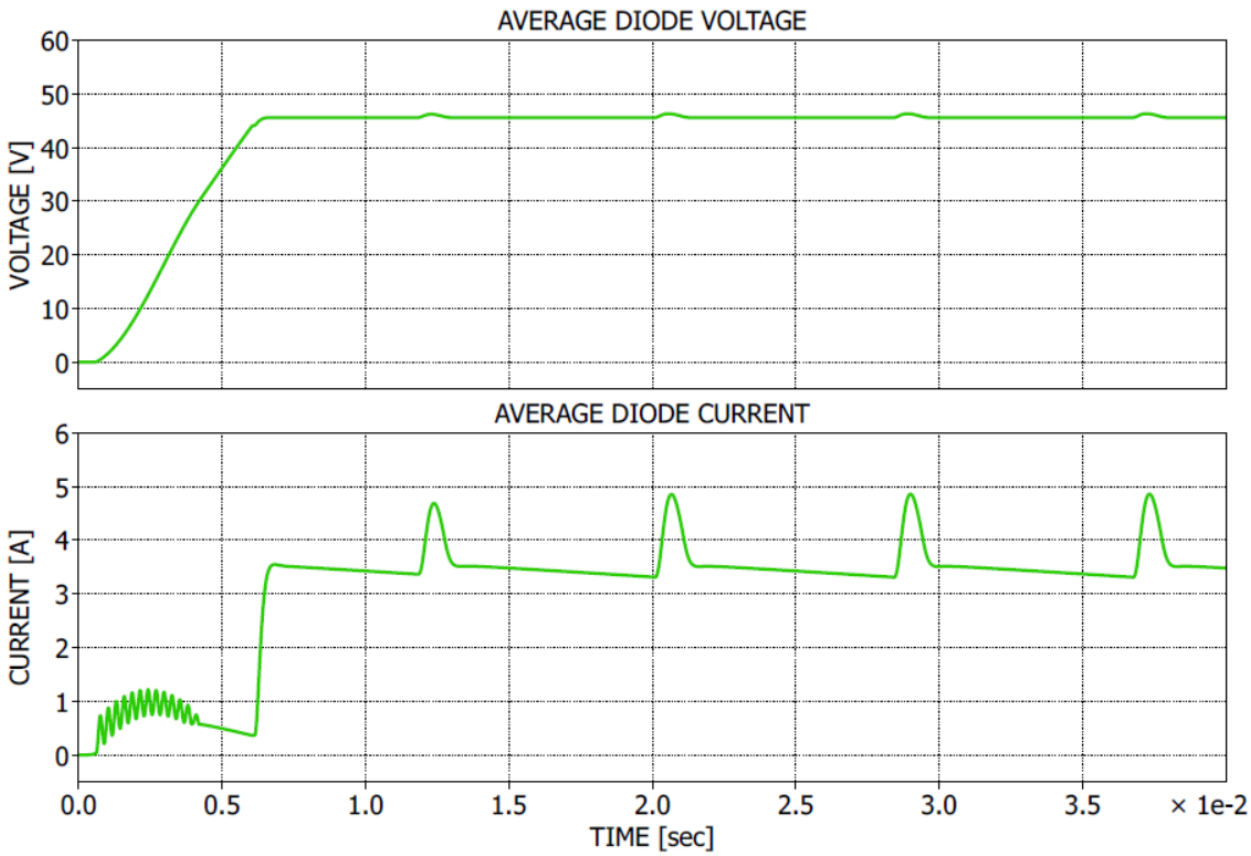

Figure 36: Average Diode Voltage and Current Waveforms

The next component worth exploring is the free-wheeling diode, which is expected to conduct with the MOSFET is OFF and block current when the MOSFET is ON. The average voltage and current waveforms for the diode appear in Figure 36. Again, the average current waveform of the freewheeling diode will be examined first. In 2.4, the maximum average diode current was calculated to be approximately 5A.

Averaging over 120Hz provides a steady-state average diode current of 3.55A. If the model is adjusted to assume the batteries are all at 3.3V when charging is initiated, the average diode current increases to 4.05A. There is some margin of error between the calculation presented in 2.4 and the bottom plot of Figure 36. The error is, however, entirely due to the conservative nature of the hand calculation and completely acceptable.

The diode as simulated is responding as expected, and the simulation results are accurate. The voltage plot at the top of Figure 36 is also as expected. It is the average voltage experienced by the diode, and it is expected to be approximately the same voltage experienced by the battery pack: a DC voltage around 45V.

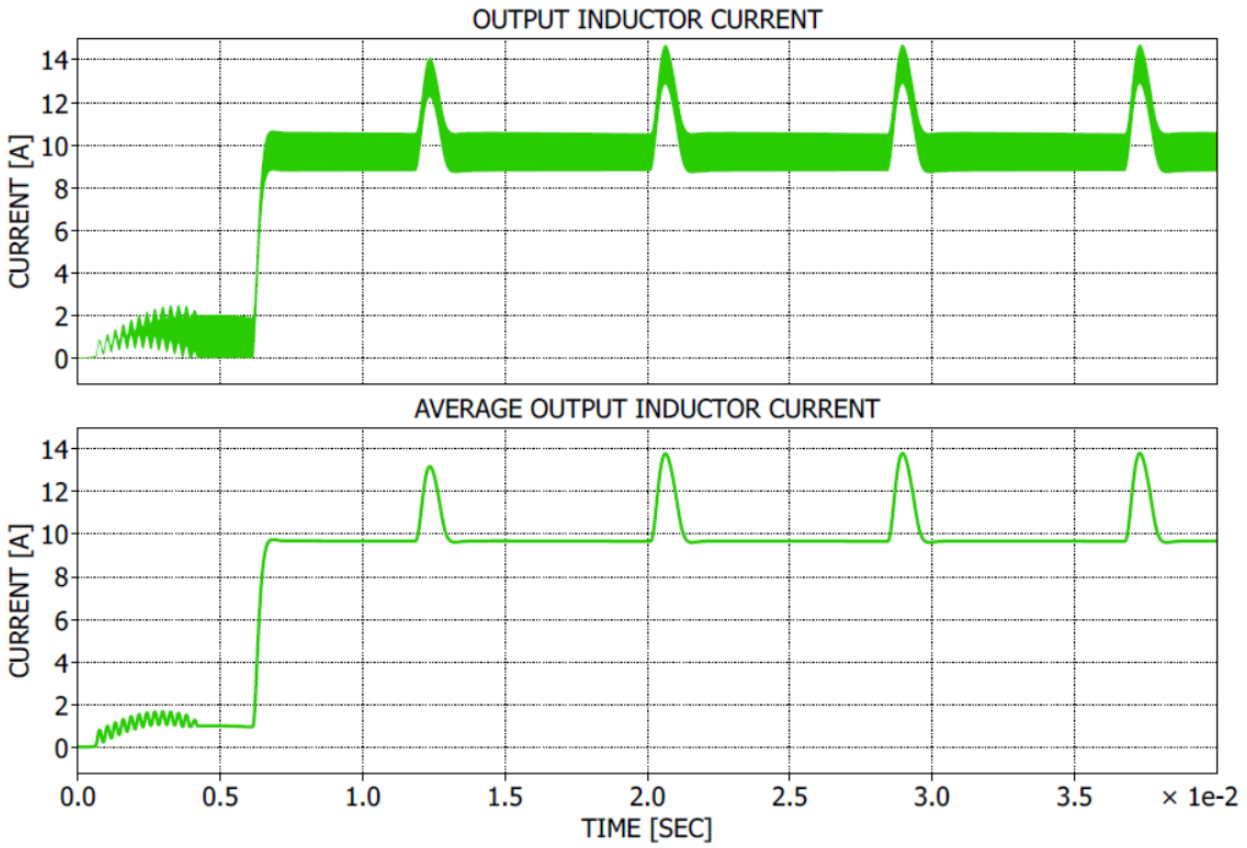

Figure 37: Output Inductor Current and Average Current Waveforms

For completeness, the output inductor current and average output inductor current are provided in Figure 37. The top plot of Figure 37 shows the actual inductor current with its ripple current. The ripple shown in the simulation is validated by the ripple current shown in the Simulink model results from Figure 27. The ripple is approximately 2A in width. The 120Hz ripple is not present in the Simulink results, because the input to the filter was modeled as a pure DC voltage.

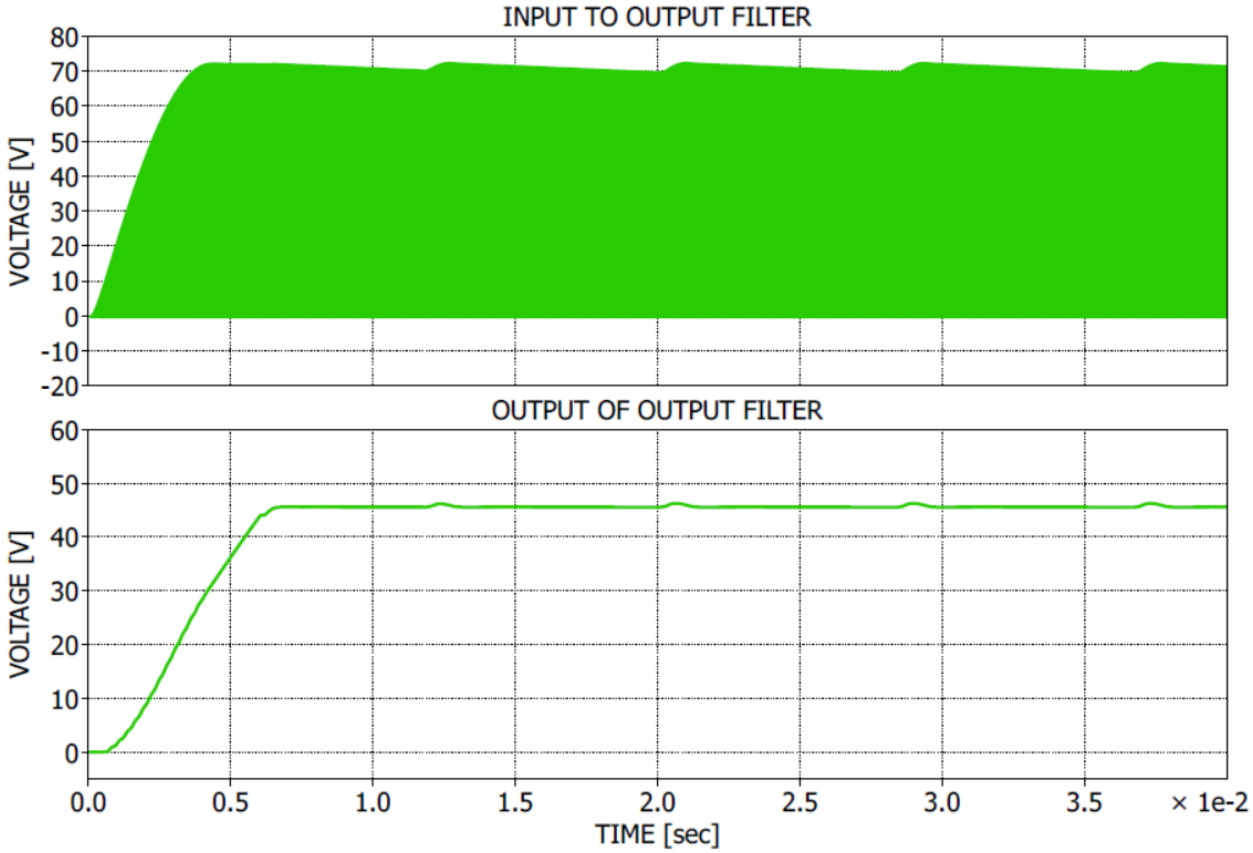

Figure 38: Output Filter Voltage Waveforms

The output filter voltage waveforms show the high frequency filtering effect of the implemented 2nd order filter. The input voltage waveform, shown in the top plot of Figure 38, is in reality a long train of voltage pulses corresponding with the switching frequency and the duty cycle. When the MOSFET is ON, the input voltage is passed directly to the output. When the MOSFET is OFF, the freewheeling diode conducts, and the voltage seen at the input to the filter drops to ground (0V).

There is a high frequency component to this waveform that the filter removes, as shown in the bottom plot of Figure 38. The filter averages the voltage signal as well, resulting in a reduction of the peak voltage from approximately 70V to 45VDC. The 120Hz ripple is still present, as expected, manifesting itself as a slight bump in the output voltage waveform. This voltage is delivered to the battery during the charging cycle.

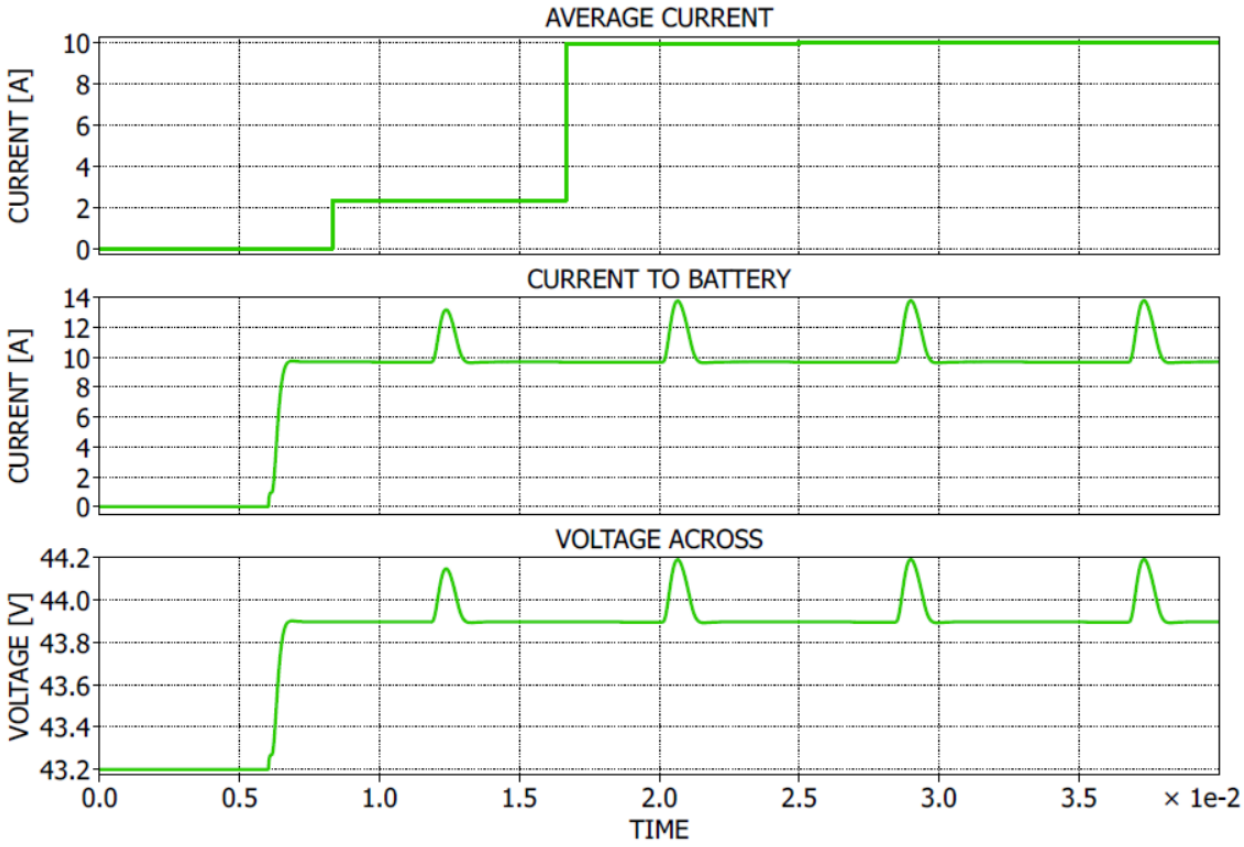

Figure 39: Battery Pack Current and Voltage Waveforms

Figure 39 shows the current delivered to the battery averaged over the period $\frac{1}{120Hz}$ in the top waveform. It also shows the instantaneous current and voltage waveforms. Peaks in the instantaneous current and voltage correspond to the 120Hz voltage ripple present in the converter input voltage waveform.

Two aspects of Figure 39 are important for understanding the simulated performance of the charging circuit. First, the average current delivered to the battery reaches the desired 10A regulated current within approximately 17ms of charge initiation without overshoot. The fact the average current does not overshoot 10A indicates the battery pack will not be unduly stressed during the 10A charging evolution. The battery cells are rated for a 10A charging current. Second, the instantaneous current peaks of approximately 13A (over 12A for less than 1ms) meet the established design requirement of not greater than 14A at any time during operation. The battery can handle this slight variation in the output current because average current is still 10A, as illustrated.

An interesting simulation to run is to change the input AC frequency to 60kHz. The rectified input will contain a voltage ripple of 120kHz, which should be filtered out by the low-pass input filter. Changing nothing else but the input frequency of the power source to 1MHz, the battery current waveform becomes the waveform shown in Figure 40. The peaks in the current are completely eliminated, and the current never overshoots 10A, which is excellent for the reliability of the battery pack over extended use and cycling.

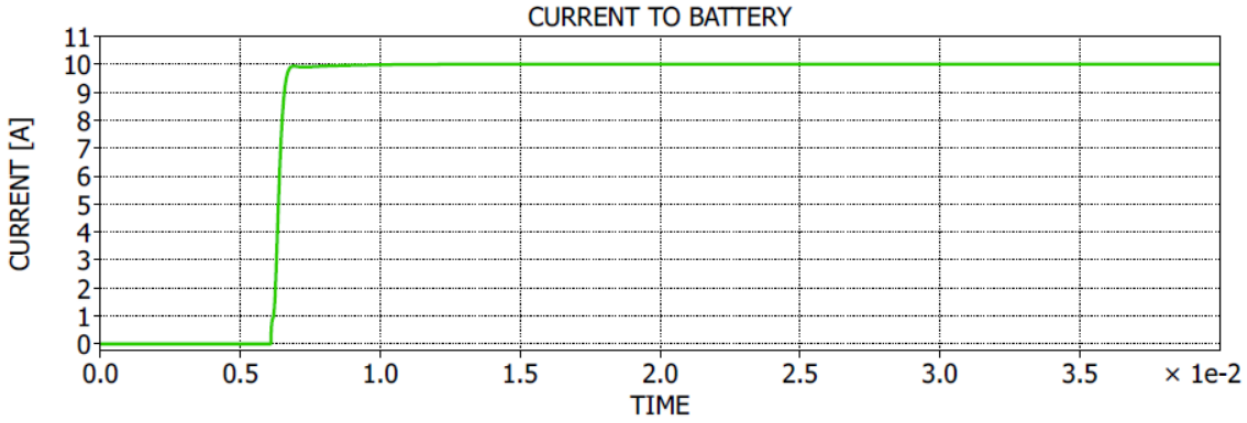

Figure 40: Instantaneous Current to Battery with a 1MHz AC Input

6.3. Transient Response Analysis

The analysis of any power converter would not be complete without a validation of input and output transient performance. In this case, there are three particular transients of concern. First, the on-off transient is of interest. Already, the "on" transient has been provided, as seen in Figure 39. The "off" portion of the transient must also be simulated and observed.

The second transient of interest is that of a voltage spike at the battery pack terminal. The final is an output voltage drop again at the battery. Both are simulated in a worst case scenario.

The transient analysis of the system was performed via simulation. Experimental results should be obtained as possible to validate the results. The system was turned on at time 0 and allowed to reach steady-state prior to initiating the transient. At time 0.015s, the transient was initiated for all cases. Voltage transients were based on the expected 39.6V to 43.2V operating range of the battery pack. The system is place in equilibrium at one extreme and then switched at 0.015s to the other. The transient response was then observed. The following section provide waveforms and analysis for each transient of interest.

6.3.1. Off-On Transient

The on-off transient is perhaps the most mundane transient to study. Already, the feedback has been designed to prevent excessive overshoot. When the source is removed with the system at steady-state, the circuit is expected to deplete all energy stored in electro-magnetic components and level off at zero current and the fixed voltage of the battery pack. The output voltage of the battery pack was set to 3.6V/cell or 43.2VDC for this simulation. This is expected maximum charging voltage of the battery pack. 3.7V is allowed per the datasheet, but a safety margin for actual operation has been applied. Figure 41 shows the results of the simulation.

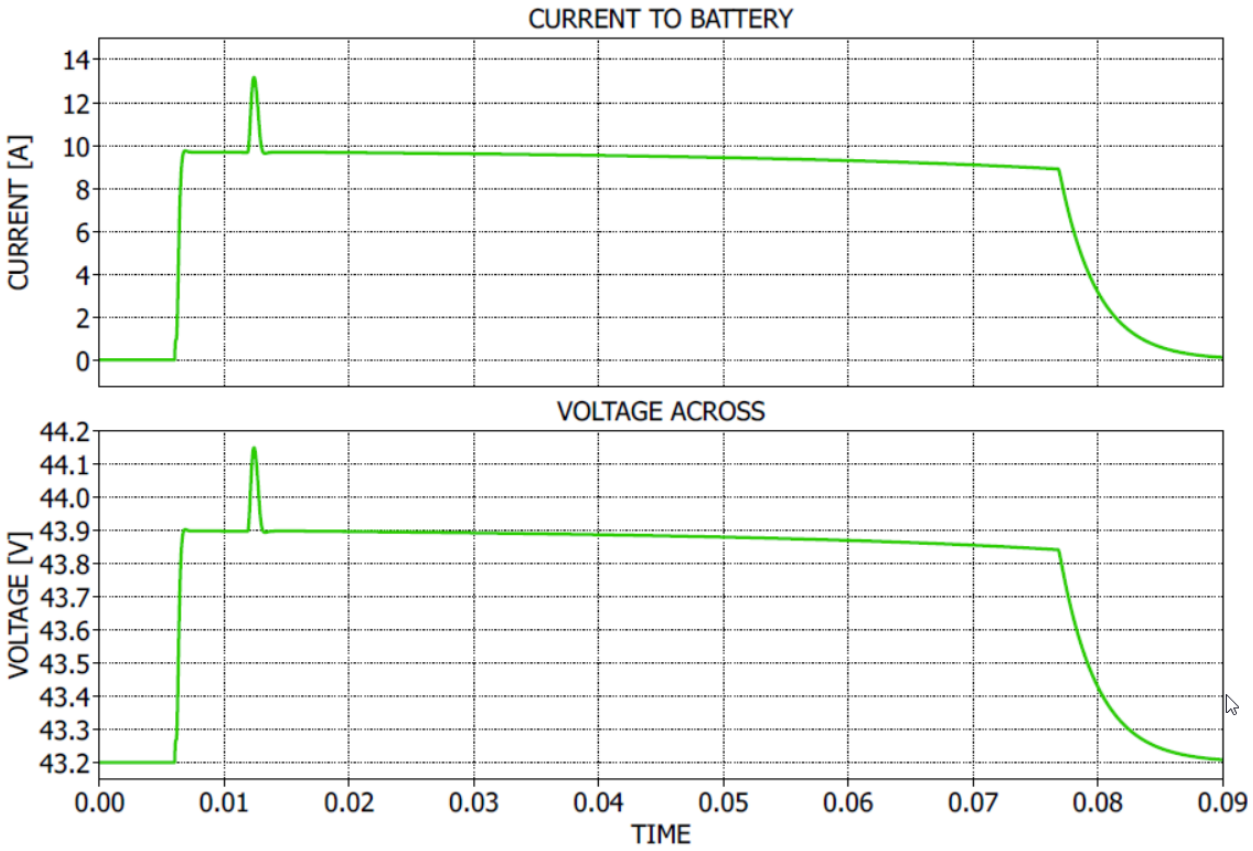

Figure 41: On-Off Transient Waveforms

The on-off transient results in Figure 41 are as expected. The source is secured at time 0.015s. The 15 µH output inductor continues to source the current as able, with current decreasing linearly over approximately 60ms. As the magnetic field collapses, the voltage and current exponentially decay and asymptotically approach the voltage of the nominal battery of the battery pack and 0A current respectively. One assumption made in this simulation that would not be true of the actual design is that the gate signal to the MOSFET would continue to operate. This assumption leads to an increase of the available energy in the system to continue sourcing the output inductor and the long linear decays of the voltage and current before exponential decay. In reality, the driver would loss power and the MOSFET would turn off, isolating the input of the converter from the output. The time lag is expected to be much shorter for the real system as a result. The general behavior, however, is expected to be the same. The on-off transient is a safe evolution that meets all the design requirements of the system.

6.3.2. Battery Pack Voltage Spike (39.6V to 43.2V)

The response of the system to either a spike or drop in output voltage is necessary to determine the safety and robustness of the system. A voltage spike is unlikely. It might, however, occur if the battery pack is failing or some other unexpected event happens.

In many respect, the voltage spike transient is a test of how well the feedback system works to correct an over-voltage condition. If battery pack voltage spikes, the current sense resistor will experience a decrease in current, because there will be a smaller potential difference between the battery pack and the output voltage of the power converter. This will cause the designed PID controller to rapidly

increase the duty cycle of the MOSFET to re-obtain an equilibrium condition. The control is not perfect or instantaneous. It will take some time for the error signal to build and the output current to regain 10A. What is good about this transient is the simple fact that current to the battery decreases. There are no large, potentially damaging current spikes for the battery pack to absorb. Instead, a steep drop in current is experienced, followed by a rapid, but controlled return to steady state. Figure 42 shows the transient. The transient is over in approximately 2ms. This transient is safe and tolerable.

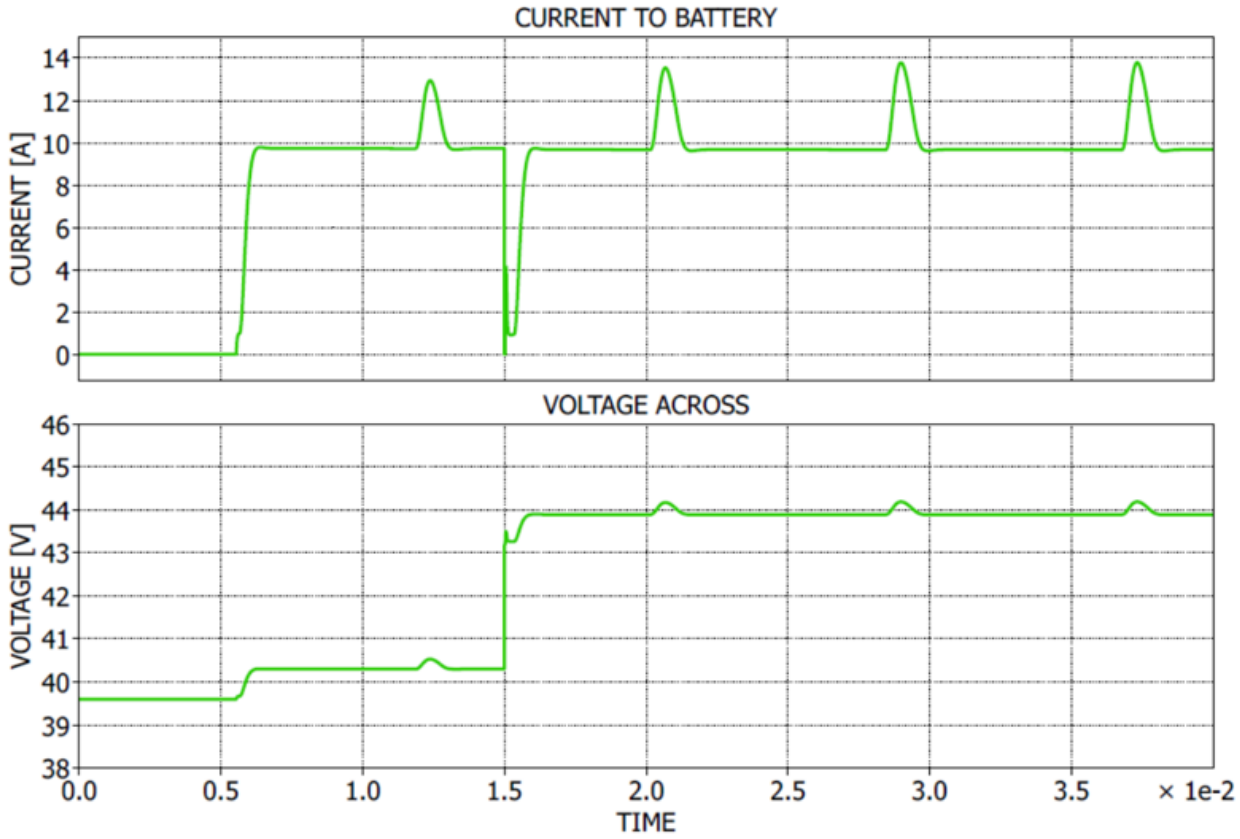

Figure 42: Voltage Spike Transient Response

6.3.3. Battery Pack Voltage Drop (43.2V to 39.6)

A drop in battery pack voltage is probably the most likely scenario to encounter in operation. A cell might fail, or a short might occur. The system will be designed to avoid these conditions, but no system is 100% safe and reliable. As the most likely transient, it is also the most danger. The simulation results provided in Figure 43 show an unacceptably large 30A peak in current as a step change in voltage occurs. This occurs because the potential difference between the output of the converter and the battery pack increases by some 3VDC and the ESR of the pack is very low. Ohms Law dictates the raise in current. What is interesting, however, is that the transient occurs very rapidly. The peak is immediately reined in by the ability of the output inductor to actually provide that current. It physically cannot, and so a more gradual peaking of the current appears in the waveform, which is arrested by the feedback at approximately 24A.

The battery pack can handle this transient so long as internal voltage of the individual cells is not pushed much over 3.6VDC. The real issue with high current is heating of the individual cells. If the heat is removed from the system, then the cells can in fact be charged at a high current rate.

The problem with this transient resides in the fact that it unnecessarily and dangerously stresses the battery cells. Also, a lower limit of 36.9VDC was used for this analysis because it is the lower limit of the battery pack's operational limit, but if the voltage were to drop lower, the transient would be more several. For this reason, it is worth exploring options for limiting the peak current.

One possible approach is to program the control to secure the MOSFET and reset when a current above a given threshold is experienced. This threshold might be as low as 15A or as high as 30+. Experimentation in the lab is required to fine tune the set point for maximum reliability and safety. Securing the MOSFET by grounding the gate pin effectively forces the system into an "off" transient, protecting the battery pack from damage resulting from the power converter. Of course, if a short in the battery pack was the cause of the voltage drop, excessive discharge current or fire might still damage the battery pack. The smart engineering solution, however, is to secure the system, assess the problem, and resume charging only once the problem has been corrected.

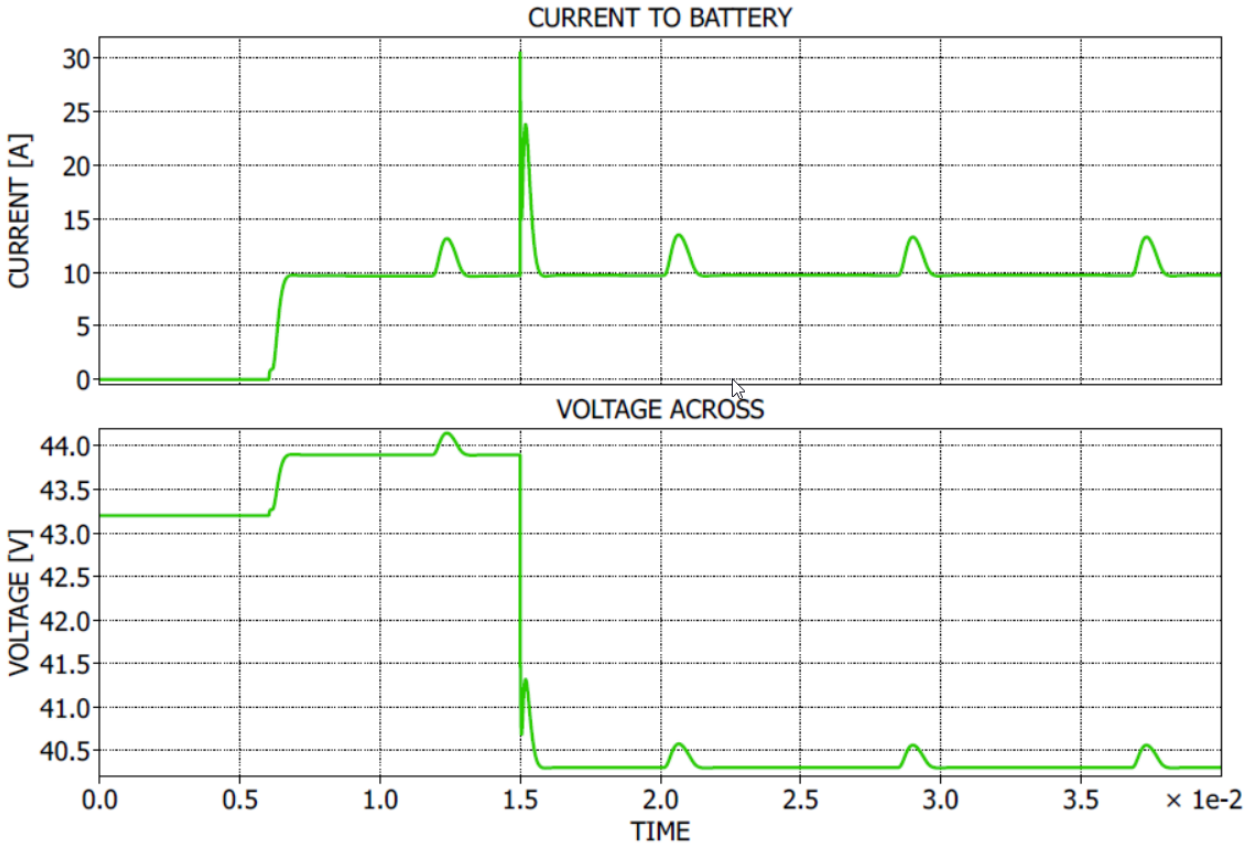

Figure 43: Voltage Drop Transient Response

7. PCB Design & Circuit Layout

All design fabrication efforts were accomplished in Cadsoft® **E**asily **A**pplicable **G**raphical **L**ayout **E**ditor (Eagle) 6.5.0 Light. Another software tool could have been used. One package that was explored was ExpressPCB. ExpressPCB is a very basic PCB design tool. It was ultimately rejected, because the ability to define custom pad layouts was limited and difficult. The final circuit has quite a few custom pad layouts, which made ExpressPCB a poor choice. The designer was not familiar with Eagle prior to this project.

Eagle Light is a free PCB design tool. It contains a rather extensive library of predefined devices and supports to development of custom packages. The program was not the easiest or most user-friendly solution, but it is one of the most full-featured. Eagle Light does have some limitations. The board is limited to two layers and a size of 100mm x 80mm (3.94in x 3.15in). Fitting all the circuit components into this size constraint was a challenge, but it was accomplished.

The first step in the PCB design effort was to build the schematic in Eagle with all the circuit components and signal paths represented. Figure 44 shows the complete Eagle circuit schematic. Many of the features of the design that were not present in the PLECS® model necessarily appear in the Eagle Schematic. In particular, the components for the MOSFET driver circuitry and BJT-Zener diode regulator circuit are included. Also, the Eagle schematic included individual components as they would appear in the circuit. Lumped capacitance shown in Figure 31 had to be separated out to account for individual capacitor placement on the PCB.

While building the Eagle schematic, a lot of effort was expended defining custom pad layouts for individual circuit components. For example, the 2.3:1 transformer at the front end of the circuit is actually a large toroid transformer with 2 sets of leads that can be wired in series or parallel. The design decision to use size 6 machine screws to secure the input and output leads to the PCB required a custom pad layout to be designed and associated with the transformer symbol shown in the schematic.

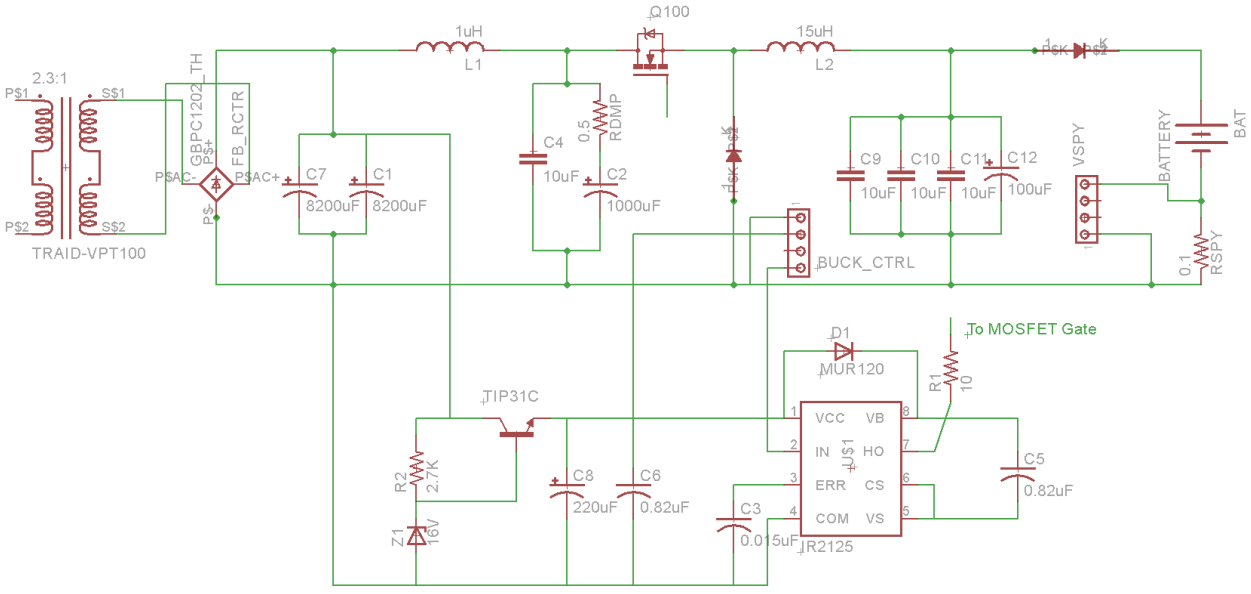

Figure 44: Eagle® Schematic of Buck Converter

Several circuit components required custom packages in addition to the transformer. The full-bridge rectifier, both inductors (L1 and L2), the diodes, and the battery terminals were all custom packages for this application. The full bridge rectifier was a particular challenge, because the original device chosen for the project came with blades. The idea was to push the blades through the board, solder them in place, and then use the blades as test points for performance evaluation. This approach was abandoned when price quotes more than doubled for a PCB with cladded rectangular holes instead of standard through-holes.

The finalized schematic included all the components to be placed on the PCB and their associated packages. The original PCB design for the converter failed to incorporate the drive circuitry into the board. Initial testing of this preliminary design included the drive circuitry built on a breadboard with gate signal and ground wires between the PCB and the breadboard. Excessive inductive ringing of the gate signal during operation resulted in ineffective switching of the MOSET, poor power transfer, and unexpected failure of the MOSFET in addition to a variable, uncontrolled voltage output at the battery terminal. Including the drive on the PCB corrected this issue and result in much improved converter performance.

Placement of circuit components on the PCB was a design challenge. Some of preliminary concerns were signal interference from the AC input to the DC output, high power and current limitations on the PCB traces, and heat dissipation. A ground plane was introduced under the DC components of the circuit upstream of the smoothing capacitors to address potential AC-DC signal interference. PCB traces were purposefully made as wide as possible to address the high current issue. With wider traces, less I^2R losses in the traces are expected at high power operation.

Additionally, while the prototype features 1.0oz copper traces, the final production design should include 2.0oz copper. The decision to use 1.0oz copper was made to limit the cost of the prototype board. The final board will be bought in sufficient quantity to make the 2.0oz copper affordable. Additional, 2.0oz copper is the correct rating for the desired 10A output current. 1.0oz copper is sufficient for the rest of the circuit.

Finally to make room for heatsinks and to physically introduce some separation between components with heat dissipation requirements, the MOSFET and the BJT were placed on the backside of the board. The idea is that the board will almost certainly be in contact with the metal end cap of the AUV, which is also in contact with the AUV hull and seawater. Heat can be dissipated through the end cap and transferred to the sea water effectively and reliably during the charging process. In this configuration, not only is the charging circuit mechanically secured inside the AUV, but the need for individual heatsinks is eliminated and space is preserved while heat is still effectively dissipated. Design efforts at this stage of testing and development did not include packaging constraints or volume optimization beyond what has already been discussed.

Figure 45 shows the physically placement of components on the topside of the PCB. The board dimensions are 100x400mm. This is the maximum size supported by the free version of Eagle®, and it was a challenge to fit everything. From right to left, progression of the power can be followed from input to output. AC power comes in on the lower left-hand of the board. It is rectified and smoothed, filtered, and then sent to the converter cell. The output appears in the lower right-hand corner of the board.

The most important observation of the PCB design is that the rectification and smoothing requires such a large percentage of the board layout. This is due to testing using 60Hz. Much of this space can and should be reclaimed for the final AUV design, optimized about the mean final input frequency. If 1MHz is assumed, the large smoothing capacitors can be completely removed. The input filter would be sufficient to completely filter out this frequency, saving approximately 30% of the layout space of the board.

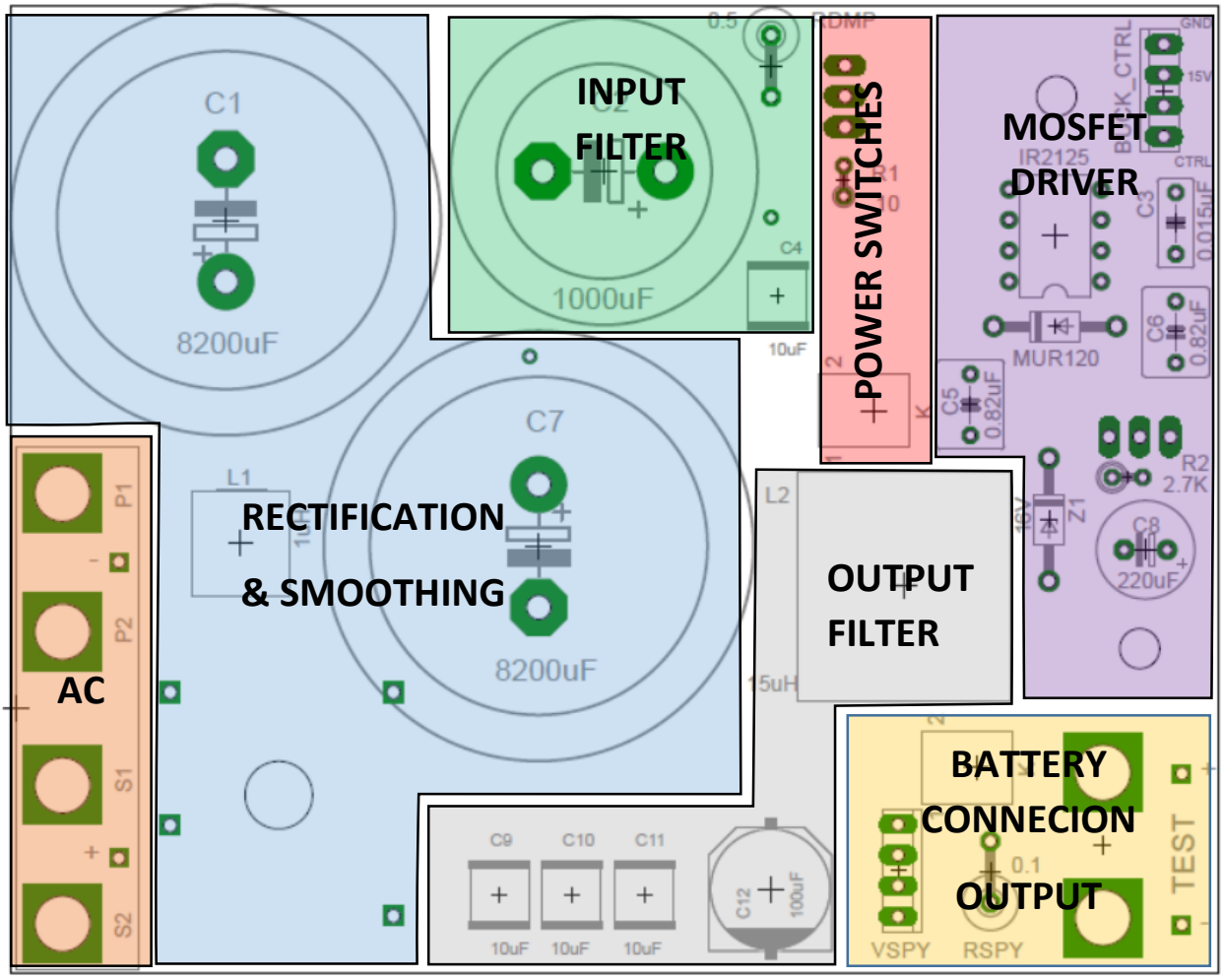

Figure 45: Eagle® PCB Design: Component Placement

The routing of traces was done by hand. While Eagle® does include an automated feature for this process, the desire to widen traces drove the decision to manually route all traces. Traces were thickened whenever possible to minimize I^2R losses and board heating during operation.

A ground plane was also added to the top of the board, as illustrated in Figure 46. The ground plane assisted the design in two ways. First, it made connecting components to ground easy. Second, it permits the large return current from the converter to flow with little voltage drop, increasing the performance and reliability of the design. The ground plane was not extended over the entire board to prevent coupling of the ground plane with AC frequencies; only DC components lay above the ground plane.

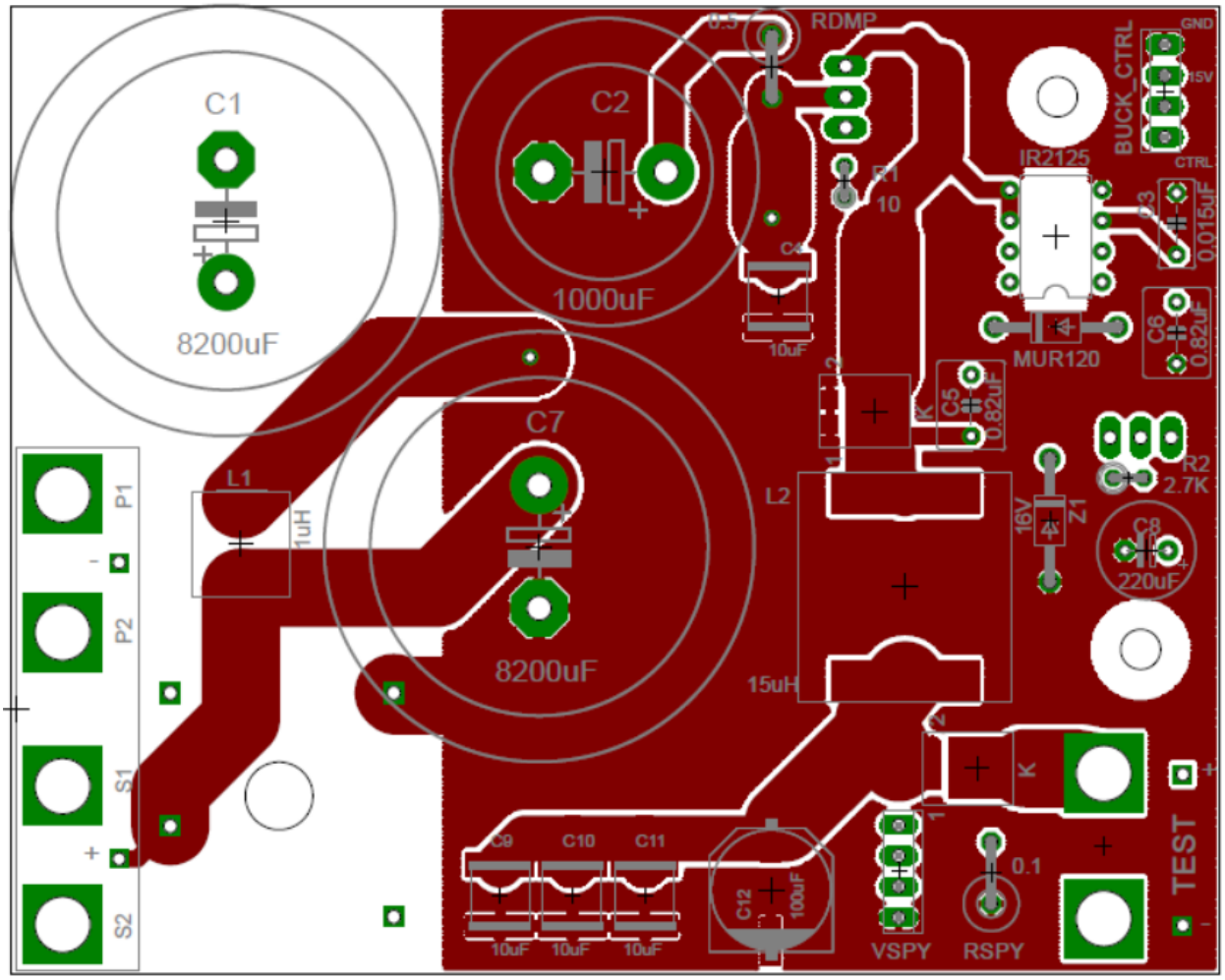

Figure 46: Eagle® PCB Design: Top Side Traces with Ground Pour

The board of the PCB is less populated with components and traces (Figure 47). However, the primary heat-dissipating components were placed on the bottom to permit easier mounting of heatsinks. The full-bridge rectifier, the MOSFET, and the BJT were placed on the bottom of the board for this reason.

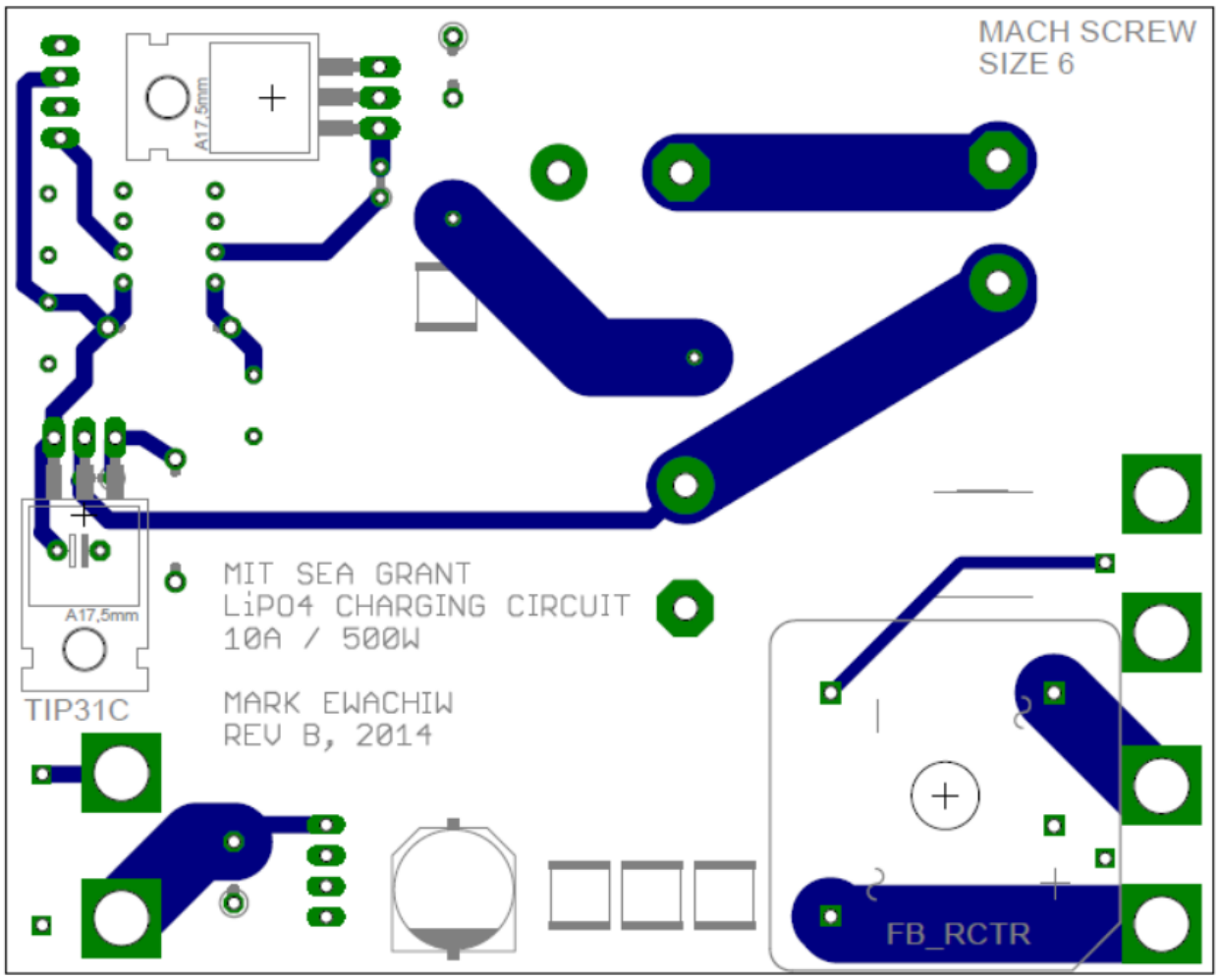

Figure 47: Eagle® PCB Design: Bottom Side Traces

In general, the PCB design is rather uninteresting. With the exception of the extra-wide traces, standard design practices were followed and a reliable vender chosen for production. The challenge in this part of the project centered more around learning the software package and fitting everything on the board nicely. Room exists to improve the layout, as mentioned, especially once the final input frequency range is well-understood and specified.

The PCB design files are available upon request from the author, along with all Gerber files that may be required.

8. Results and Conclusions

The PCB as specified was outsourced for fabrication, populated, and tested in a lab environment. The parts list is included for reference in Appendix A: Parts List. The DC-end of the converter (upstream of the full bridge rectifier) was initially tested using lab power supplies in series as needed. Additional higher-power tests incorporated the use of a standard two-prong electrical cord plugged into a standard North American 120VAC, 60Hz electrical outlet. These final tests confirmed the end-to-end performance of the entire system.

Testing was not without its challenges. Initial efforts focused solely on validation of specific functional blocks of the circuit and rating validation. It was important to validate that each functional block was performing properly. It was also equally important to ensure the system could handle the rated the intended voltage and current loads without failure. Troubleshooting was conducted as appropriate.

Operation of the converter was tested using a 10% and 50% fixed duty cycle with a fixed load and no feedback over a full spectrum of input voltages up to approximately rated voltage. These tests allowed validation of operation prior to attaching the variable load of the battery. Additional testing increased the duty cycle and input voltage to boost the output power slowly into the design range. Finally, the circuit feedback algorithm controlled by the PSOC®5LP was incorporated into the system and tested. Adherence to the desired current level, which was varied for testing, was observed using the voltage across the sense resistor and an oscilloscope.

8.1. Functional Block Validation

After board population, the immediate testing efforts were focused on validation of key functional blocks. Figure 45 provides an excellent illustration of the principal functional blocks of the overall circuit. Filters were not of immediate concern, because they are comprised of passive components with very little potential for failure if operated within voltage and current ratings. As a results, most of the testing effort involved validating the performance of the rectification block, the MOSFET driver, power switches, and the battery connection output with its current sensing resistor. As much as possible, each block was isolated for the purposes of validation. All attempts were made to minimize damage to the board and components during preliminary testing.

8.1.1. Rectification & BJT-Zener Voltage Regulator Testing

The operation of the rectification and smooth block was straightforward and easy. This particular test require the use of the transformer, a power cord, and a standard North American electrical outlet. The cord was connected to the transformer and tested to provide an acceptable output voltage AC signal.

An approximately 52VAC signal was observed on the output of the transformer, indicating a proper 2.3:1 turns ratio reduction in the voltage. With the voltage confirmed, the transformer's output was connected to the input of the PCB and the full-bridge rectifier. The converter was not operated. The source of the MOSFET was tied to its gate to ensure V_{GS}=0 and that the MOSFET would be hard off at all times. The output DC voltage of the smoothing capacitors was observed to be a stable 72VDC as expected.

During rectification testing, the BJT-Zener Diode voltage regulating circuit of the MOSFET driver functional block was also tested. The input voltage to pin 1 of the IR2125 was observed to be 15VDC as expected, confirming that the voltage regulating circuit was working as anticipated.

These initial tests are rather mundane in that they do not shed any real light on the important questions at hand. Precisely, the do not answer the questions:

- Does the convert work as designed?
- How well does it work? What is its efficiency?

The converter, however, will not work as intended if these basic elements fail to provide the required input power necessary to a) power the control circuitry, and b) provide input power to the converter.

Initial testing determined that rectification and the BJT-Zener voltage regulator performed as expected. After testing, the transformer was removed from the system and testing continued with the use of lab DC power supplies for the additional safety offered by these devices.

8.1.2. IR2125PBF MOSFET Driver Testing

The IR2125PBF MOSFET driver's functionality is essential to the proper switching of the floating MOSFET. Several issues could prevent the driver from properly switching the MOSFET. The prevalent certain on testing was that the BJT-Zener regulator supplying the driver might not provide enough current to properly charge the bootstrap capacitor at a selected switching frequency of 600kHz. The BJT-Zener regulator was chosen to prevent this from being an issue, but testing was required to confirm performance.

Initial testing with the driver circuit was a failure. In the first iteration of the PCB, the IR2125PBF driver circuit was not integrated into the PCB. It was instead built on a proto-board and the output was feed over a 12" long wire the gate of the MOSFET. Inductive ringing during operation of the converter resulted in excessive cycling of the MOSFET and component failure. More than a handful of MOSFETs failed during a series of unsuccessful tests. The solution to this problem was to modify the PCB to include all components of the IR2125PBF driver circuitry, including the BJT-Zener voltage regulator, as suggested by the application notes [27].

The second prototype PCB, which decreases the trace length from the output of the IR2125PBF driver to the gate pin of the MOSFET to less than 1", resolved the driver performance issue. The IR2125PBF performed according to specifications over a series of different voltage inputs (up to rated voltage) without issue or failure. Additionally, the MOSFET was observed hard switching "on" and "off" at 600kHz with duty cycle ratios ranging from 10% to 85%. V_{GS} was consistently a 14-15VDC, as designed.

As expected the MOSFET driver did not work with a DC input voltage of anything below approximately 12VDC. Less than 12VDC, the driver IC does not have enough voltage to operate properly and an output signal was not observed. At 15VDC, the driver will function. However, the system was not designed to operate that this low voltage. Input voltage is intended to be in the 70-75 VDC range.

The successful testing of the MOSFET driver at moderate input voltages (30-50VDC) permitted further testing of the converter's overall performance and efficiency.

8.2. Converter Performance & Efficiency

Validation of component performance at rated voltage was absolutely essential prior to performing full-power tests. DC input voltage up to 75VDC was provided by lab DC power supplies. For these tests, the PSOC 5®LP was provided either an error signal from its onboard digital high (or low) voltage to force the

control algorithm to drive the duty cycle to its setup maximum or minimum percentage. This was done for two reasons. First, a fixed duty cycle was desired to easily and quickly determine if the output voltage followed, as expected:

$$V_{out} = D\,V_{in}$$

The output should, therefore, be constant and proportional to the input voltage when applied across a fixed resistive load.

Second, it was desirable to determine if the control algorithm was at least functioning on some nominal level. With a fixed high error signal, the controller should push the duty cycle to its minimum limit. With a low error signal, the controller thinks the output current is too low and pushes the duty cycle to its maximum limit. This functionality was verified prior to connecting the controller to the converter MOSFET driver input. Its operation in it prototype was validated during these two tests.

The first test used a 50% duty cycle and a 10Ω load resistor. Efficiency was calculated using the input current and voltage provided from a DC power supply and the reading of the output voltage developed across the fixed load resistor. The test setup is provided in Figure 48.

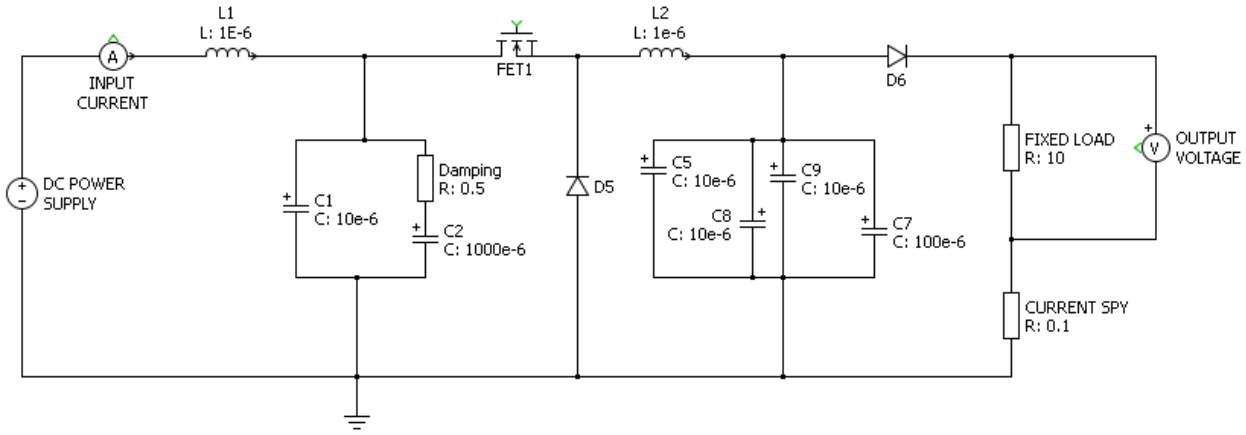

Figure 48: Lab Test setup for Efficiency Calculations

Voltage was increased to 38VDC – the limit of the DC power supply – and the output voltage and efficiency of the converter were observed. The results of this test are in Table 2.

Table 2: Converter Performance with D=0.5 and Variable Input Voltage

V_{in}	I_{in}	V_{out}	P_{in}	P_{out}	η
5	0.05	0.0	0.3	0	0%
10	0.08	0.0	0.8	0	0%
15	0.48	7.3	7.2	5.4	75%
20	0.63	10.0	12.6	10.0	79%
25	0.78	12.6	19.5	15.9	81%
30	0.93	15.2	27.9	23.1	83%
35	1.07	17.8	37.5	31.7	85%
38	1.16	19.3	44.0	37.2	85%

While the output power of this initial test is more than an order of magnitude lower than the converters rated 500W, the data in Table 2 does provide some valuable insight into the performance of the converter.

First, the output voltage is 0VDC when the input voltage is less than 15VDC. The reason for this is discussed in 8.1.2. The MOSFET driver IC is underpowered and not providing a switching signal to the MOSFET gate. Above 15VDC, the output voltage is almost perfectly half the input voltage. This result shows excellent duty cycle regulation of the output voltage, which is an indication of proper, proportional switching of the MOSFET.

Second, the efficiency η is important to note. This power delivered to the load resistor did not exceed 40W is this test, however, the efficiency is observed increasing as the input power increases. 85% efficiency at this low power is a respectable performance level. The converter is operating outside of its intended operational range, yet its efficiency is still rather high.

One important reason for the efficiency being less than calculated in Chapter 3 is that the converter itself has some overhead losses associated with it operation at any level. The most important examples of overhead losses in the converter are the BJT-Zener voltage regulator and the sense resistor. The BJT-Zener voltage regulator losses increase proportional to input voltage up to approximately 6W, as shown in 5.2. The sense resistor dissipates power proportional to the square of the current delivered to the load. Overhead losses make efficiencies determined while outside of the intended operational range difficult to evaluate and gain insight from. Qualitatively, however, the converter is expected to perform at a higher efficiency when delivering more power to the load. Figure 47 provides a graphical appreciation of the data provided in Table 2.

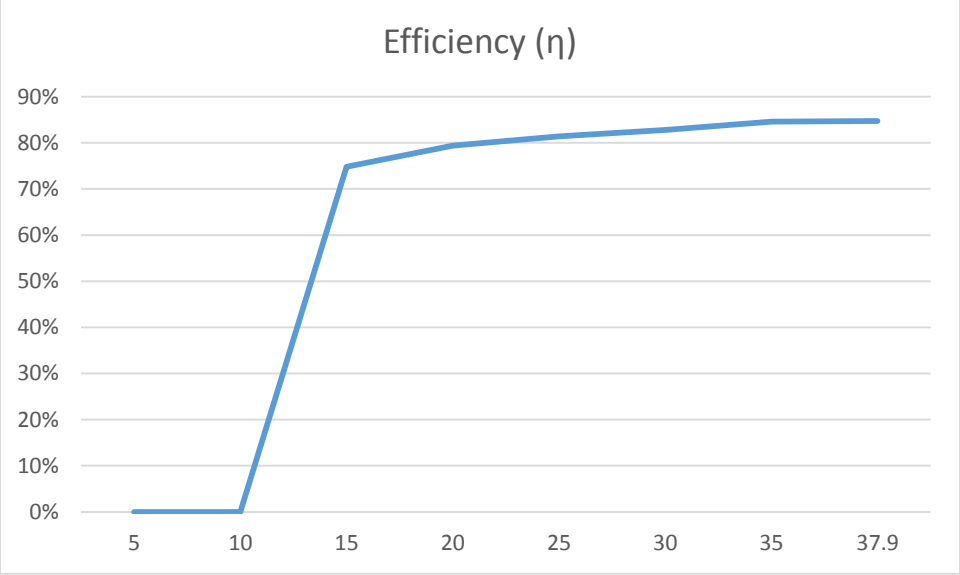

Figure 49: Converter Efficiency with D=0.5 and Variable Input Voltage

The second set of tests conducted were intended to validate performance at the intended operational voltage of approximately 70VDC. The duty cycle was driven to its lower limit of 10% by providing a digital high sense voltage to the input of the controller. The input voltage was then increased to 69V –

the maximum of two DC power supplies in series – and the output voltage measured. The output load was again a 10Ω power resistor. Table 3 provides the results from the second set of experiments.

Table 3: Converter Performance with D=0.1 and Variable Input Voltage

V_{in}	I_{in}	V_{out}	P_{in}	P_{out}	η
40	0.17	4.65	6.8	2.16225	32%
45	0.18	5.32	8.1	2.83024	35%
50	0.19	5.9	9.5	3.481	37%
55	0.21	6.66	11.55	4.43556	38%
60	0.22	7.37	13.2	5.43169	41%
65	0.23	7.95	14.95	6.32025	42%
69	0.24	8.57	16.584	7.34449	44%

In these experiments, we can see that the output voltage is not as well regulated. This is most likely due to fractional importance of the rise and fall time of the MOSFET drain-to-source voltage V_{DS} during switching. At 600kHz, the period is 1.67µs, of which the rise and fall time of the IR520 MOSFET could possibly be almost 10% according to the datasheet. The result is a less precise regulation of the output voltage at lower duty ratios.

The duty cycle was purposefully made small to minimize the output power. This was done primarily to avoid damaging the load resistors, which were not rated for more than 40W of power. It was also done to protect the MOSFET which was not mounted to an appropriate heat sink at the time.

Efficiency suffered during this voltage rating test, as shown in Figure 50. However, there is a clear trend towards higher efficiency with higher input voltage. Again, the efficiency data provided here cannot be taken as actual performance, as it was obtained out of the intended range of operation.

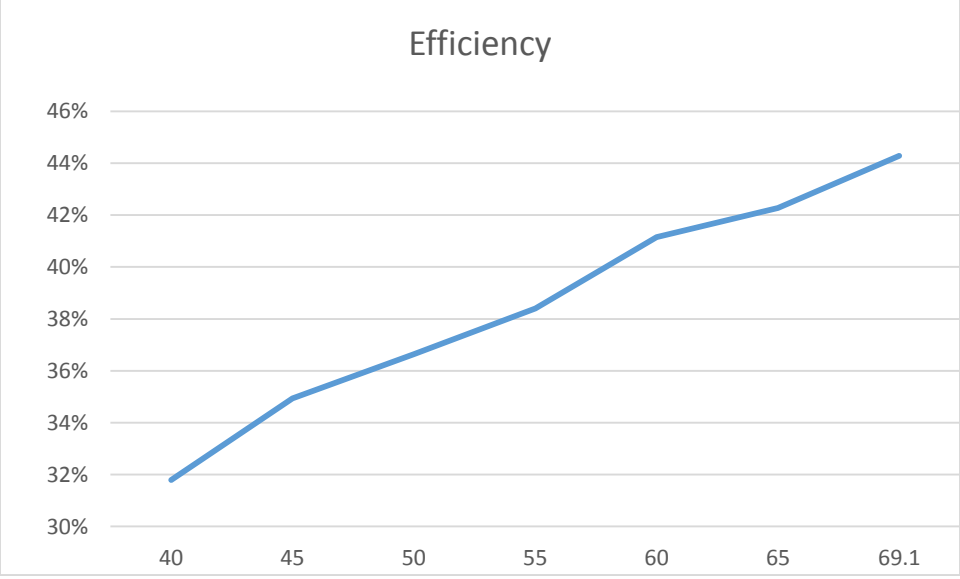

Figure 50: Converter Efficiency with D=0.1 and Variable Input Voltage

8.3. Full Power Testing

Several more test were conducted with a fixed duty cycle of 75%. The purpose of this testing was to push the converter up into its intended operating power range by varying the input voltage and observing the output. A 5Ω power resistor was used as the load resistor and the input voltage was varied in 5VDC increments from 45-70VDC. The results of these experiments are provided in Figure 51.

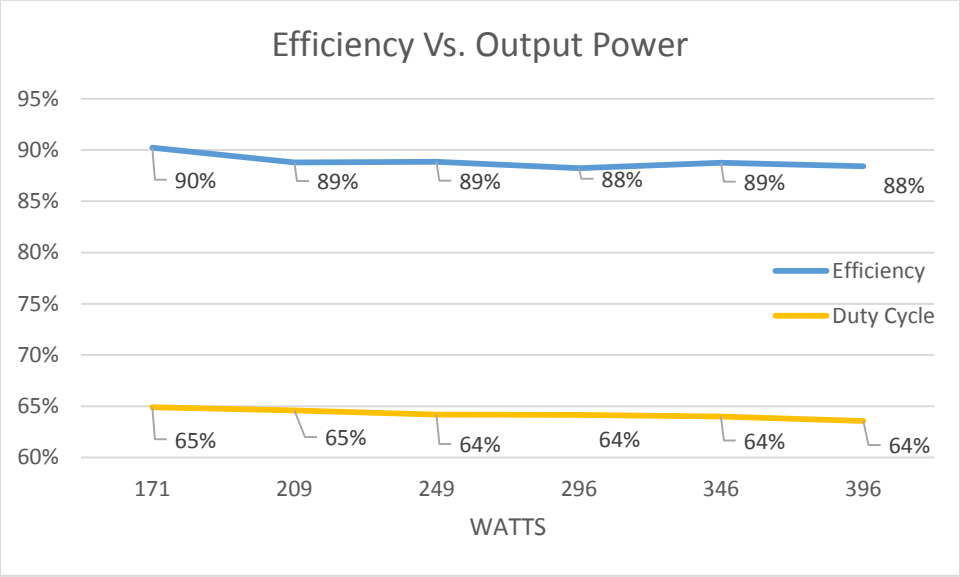

Figure 51: Efficiency vs. Power at Fixed Duty Cycle of 75%

There are three key results to note in Figure 51. First, efficiency is in the calculated range at approximately 88-89%. This efficiency is liking to fall to 86-87% when the full system is fielded because of the additional components that must be included. This result, while falling slightly below the design target of 905, is still pretty good from a performance and operation perspective.

Second, the output power is close to the desired operating range of 450W at 396W from the final data point. In this range, heat dissipation became a real problem which resulted in the failure of the MOSFET. A new heatsink has since been ordered to address the problem and correct the issue.

Finally, when a 75% duty cycle was programmed into the PSOC®, only 65-66% was observed. Again, the rise and fall times of the MOSFET were observed to affect the precision of the duty cycle. Well with the operational range of 10%-85% of the control algorithm, the precision of the duty cycle is not expected to impact the performance of the final circuit, however it is important to note.

Another test was conducted with a steady input voltage of 60VDC, a fixed load, and a varied duty cycle. The duty cycle started at 75% and was raised to 85% using the PSOC®. 60VDC was chosen because of power supply limitations. The duty cycle was raised to observe the increase in output power, the effect on efficiency, and the MOSFET switching at the higher duty cycle. The results of this experiment are shown in Figure 52. The first two data points are provided to show the consistence of the results. The final data point shows the increase in duty cycle and the corresponding increase in output power. Efficiency is constant across the spectrum of interest at approximately 88%. These results illustrate the functionality of the design.

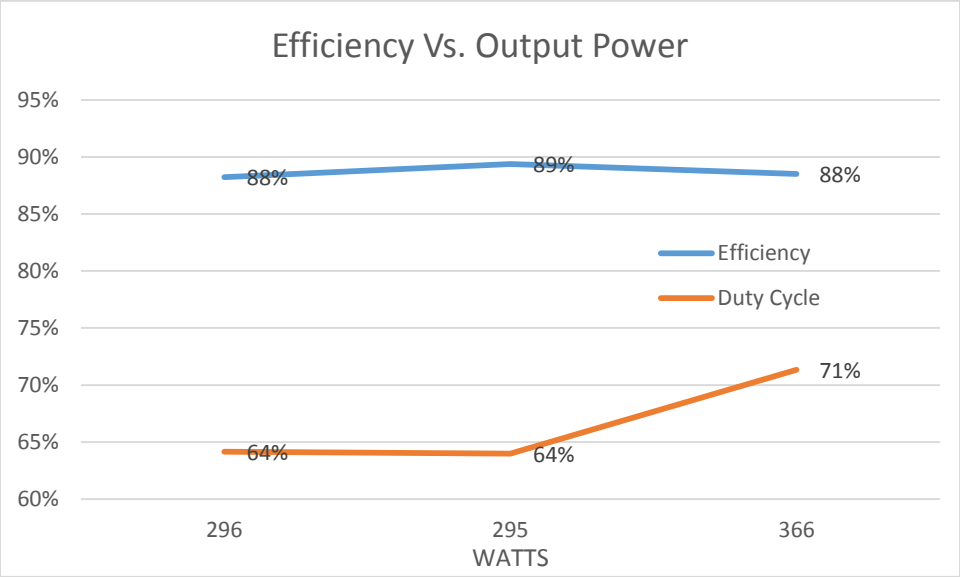

Figure 52: Efficiency vs. Power with Duty Cycle Varied

An additional test was conducted focusing on efficiency of the circuit with a fixed duty cycle of 85%. 85% is the programmed limit of the PSOC®. This limit is provided to prevent duty cycle saturation, and it was interesting to assess the effect of this limit on both actual duty cycle and efficiency at this limit. This test series pushed the design into the desired power level of actual operation, proving that the circuit could handle design loading with an acceptable level of efficiency. Two DC power supplies in series were used for this test to provide a higher input voltage. The raw data from this set of experiments is provided in Table 4.

Table 4: Fixed Duty Cycle of 85% Efficiency Results

V_{in}	I_{in}	V_{out}	P_{in}	P_{out}	η	D_{calc}
49.3	6.1	36.4	300.7	265	88%	74%
60.2	7.2	43.5	433.4	378	87%	72%
61.4	7.3	43.9	447.9	385	86%	72%
65.5	7.6	46	497.8	423	85%	70%
68.2	7.7	47.1	525.1	444	84%	69%

The final test at 68.2VDC achieves 444W of power delivered to the fixed load resistor with an input power of 525W and an efficiency of 84%. The efficiency is lower than expected and a definite dipping trend in the efficiency as output power increases is observed. This trend is shown in Figure 53. Calculated duty cycle D_{calc} is also observed to dipped, quite unexpectedly. One possible explanation for both of these observations is that the MOSFET was getting too hot during these tests. A properly rated heat sink was not available and was not being used for these tests, and so it is very likely that efficiency and observed duty cycle suffered as a result. The final data point shows the duty cycle dropping to 69%. With a proper heat sink, the duty cycle is expected to follow a more constant profile at these higher powers, like the one observed in Figure 51.

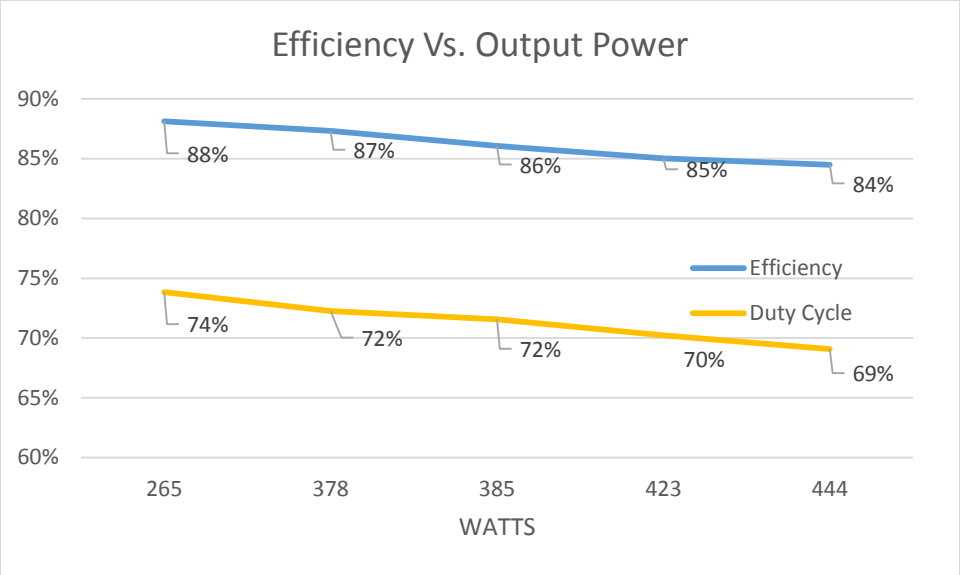

Figure 53: Efficiency vs. Power at Fixed Duty Cycle of 85%

8.4. PID Controller Testing

The final testing conducted on this design incorporated the use of the current sense. The objective of these tests were to test the functionality of the PID controller algorithm. This test was not conducted at full power. Rather than using 10A delivered to the load, 7A was selected. Reducing the power level allowed the PID controller to be tested safely and effectively while not stressing all the components in the system – especially the MOSFET. A proper heat sink had not been acquired at the time of testing, so a compromise had to be made to continue testing and achieve some level of concept validation.

7A provides 245W of power to a 5Ω load. This power level was determined to be adequate for testing the functionality of the PID controller at least for preliminary testing. PID controller testing followed the same procedure as much of the initial testing. The circuit was set up and the input voltage of the converter was set manually to 45VDC. The output voltage was then measured and the efficiency and duty cycle calculated. The input voltage was then raised at 5VDC increments until the power supply reached in maximum value. The data is provided in Table 5.

Table 5: PID Controller Test Results

Vin	Iin	Vout	Pin	Pout	Eta	Dcalc	I_{out}
45	5.4	32.58	243	212	87%	72%	6.5
50	5.7	35.2	285	248	87%	70%	7.0
55	5.2	35.2	286	248	87%	64%	7.0
60	4.8	35.2	288	248	86%	59%	7.0
61.3	4.7	35.2	288	248	86%	57%	7.0

A graph of this data is provided in Figure 54 for completeness. The first observation to make from this data is that the efficiency is steady over the range of input voltages at 86-87%. The next observation to note is that the PID controller is in fact regulating current. This is observed in both the duty cycle

decreasing as input voltage is increased and in the output current values. The desired output current was 7A. In all but the first case, the controller was able to deliver the required 7A in a very well regulated manner; the output voltage was observed to be very steady in these lab experiments.

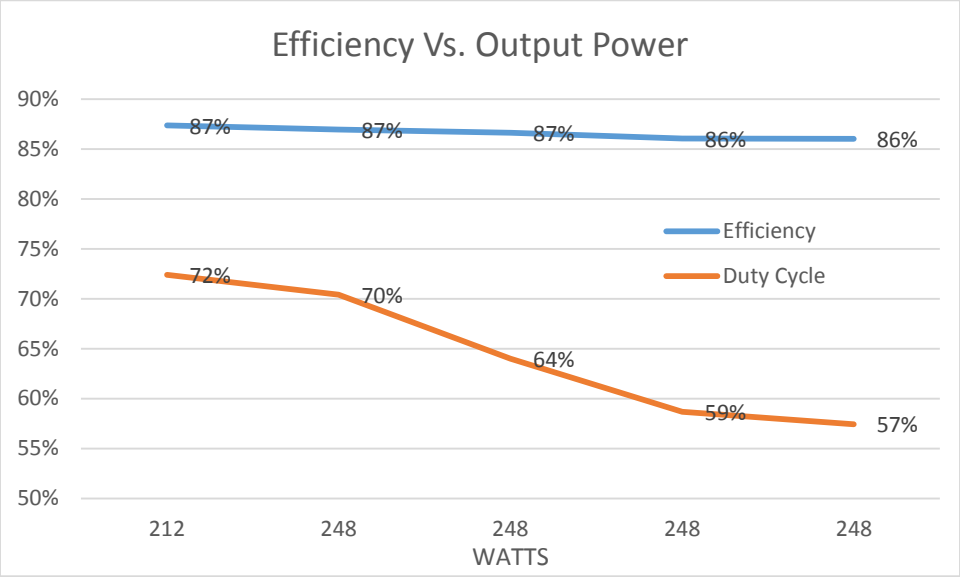

Figure 54: PID Controller Efficiency and Duty Cycle Results

The controller was observed to control the duty cycle as required. What remained unknown was whether or not it is able to do this without violating the transient requirements established in Chapter 6. The help answer this question, several "ON" transients were captured using an oscilloscope and analyzed. One such transient is provided in Figure 55. The default duty cycle was set in software to be 25%.

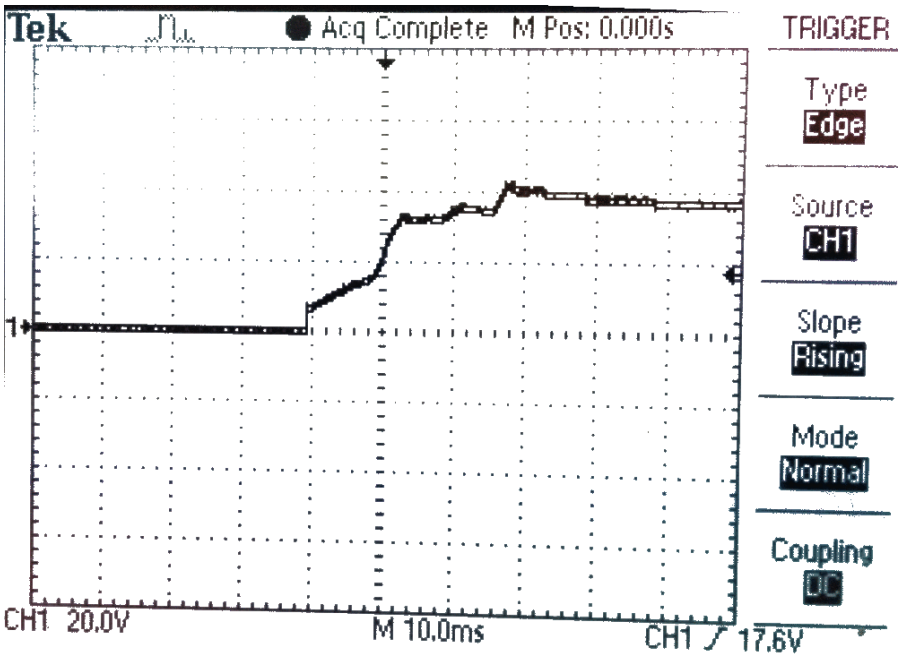

Figure 55: "ON" Transient observed using PID Controller

When the converter is powered on, the controller processes the increases in output voltage and is observed to properly regulate the duty cycle to achieve a gradual approach to the required output voltage. Some “steps” are observed. In other words, the approach is not as smooth as anticipated. This is probably related to the digital nature of the system and estimation associated with sample timing. The result, however, is quite acceptable. Very little overshoot is observed, as expected, and the output current was observed in the lab to be very well regulated at the desired current level of 7A.

8.5. Encountered Problems

Several issues were encountered during testing that need to be addressed as the project moves forward. Heat is a real concern. The MOSFET can generate some 38W of heat at full power. This heat needs to be removed from the system. Not enough engineering for this initial prototype went into properly identifying and integrating a heat sink capable of handling this heating into the design. The problem was resulted in the lab using an ad hoc heatsink. A correctly rated heatsink has been identified and ordered, but testing with it has yet to be done.

Also, a 5VDC power rail is required to provide power to the PSOC®. An LM7805 linear voltage regulator was used to supply this voltage to the PSOC®. This oversight should be integrated into the PCB in a future iteration. Using a secondary proto-board in addition to the power converter PCB is less than ideal and not suitable for final integration into the volume constraints of an AUV.

Additionally, a voltage fluctuation developed across the sense resistor resulted from the switching of the MOSFET. The voltage spike developed on the sensing line were sufficient to damage the PSOC® and prevent successful testing of the control logic. An electrolytic capacitor was used to filter the high frequency component of the sensed voltage signal. Additionally a bypass capacitor was placed across the power rails of the PSOC® to protect it from power rail fluctuations. These additions seemed to correct the problem and should be included in the next prototype.

A new PCB is recommended to properly integrate all the suggested design changes and to improve the design. Additional testing and failure analysis is required properly characterize and certify the new design for operational use.

9. Recommendations for Future Work

The work presented in this thesis represents a small proof-of-concept step towards the development of a successful wireless, underwater AUV recharging system. There are many questions left unanswered and design decision left unmade that will require additional development, study, and research. Some of this work is ongoing. The focus of future work should be on validation (testing) and integration. To that end, three primary focus areas have been identified: the power converter, the system, and the system's impact on the AUV's other systems and operating environment.

First, the power converter requires additional testing and refinement. A couple more prototypes would be beneficial to the development process. While this design effort was able to validate a baseline level of functionality, external pressures prevented the system from being fully tested and characterized at full power. Big questions that remain unanswered are:

1) How can the efficiency be improved smartly, without added unnecessary complexity and risk?
2) The current is regulated. How well is it regulated? This includes analyzing for additional transients.
3) Can the current be regulated better using a different control approach? Is a different approach needed?

There are many more. The focus of these questions are on validating and improving the performance of the converter. Ultimately, the design as presented might be good enough, but enough experimental data was not captured to provide a definitive answer to these questions. The bottom line is the system needs to be carefully evaluated for performance and reliability in quantifiable ways.

The second area of future work deals with system integration. Work at MIT SEAGRANT is ongoing to develop the battery pack and the inductive power transfer pieces of this engineering puzzle. Ultimately, the pieces need to work together to deliver energy to the AUV. Integration of these piece is crucial to the success of the final product.

There is also an integration piece that deals with the packaging of the converter into an appropriate volume and area for the AUV. Some work needs to be done to determine what that volume and area will be. The converter is intended to be housed in the pressure chamber of the AUV. This will require some careful systems engineering to ensure the heat dissipated by the converter is properly managed and dissipated. At this point, it would also be smart to establish a final energy storage size requirement to determine the number of battery cells that will be required. 5.0-5.5kWh was the range most frequency discussed, but this is subject to change.

Finally, there is real potential for future work testing the impact of an induction system on both the AUV and its internal sensors and components as well as the operating environment. Some preliminary research was conducted for this thesis using COMSOL® Multiphysics to model a nominal AUV in a saltwater environment. Transmit and receive coils were inductively coupled in close proximity to the AUV and the effects modeled. This modeling effort was not the focus of this particular work. As such, it was left incomplete.

However, there are still many unanswered questions concerning the impact of very strong magnetic fields transferring kilowatts of power on onboard electronics, navigation equipment, and sensors. It

would be a shame to successful charge an AUV inductively with this system only to have it fail and be lost at sea afterward.

Finally this project is in need of an automatic tuning feature for the induction coils. Already, lab results have shown that ability to transfer power over distance is closely related to the quality factor Q of the system and resonance. Both change slightly with distance and orientation of the coils in saltwater. Developing an automatic tuning circuit which would be capable of zeroing in on the resonance peak of the system given its distance and orientation would greatly assist in the development of a truly efficient power transfer system.

It should be clear from this list of future work that the project is far from over. There are many opportunities for future research and development. The list provided contains some highlights and more immediate topics of interest, but it is not meant to be all-inclusive or final. Certainly, as the project progresses more questions and challenges will arise that will require hard-working, talented engineers with innovative solutions and more than a little persistence.

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Appendix A: Parts List

COMPONENT / SPEC	MANUFACTURER PART #	ADDITIONAL SPECIFICATION
RECTIFICATION		
INPUT TRANSFORMER (2.3:1)	VPT100-5000	115VAC INPUT; 5A OUTPUT
FULL BRIDGE RECTIFIER	GBPC1202	200V 12A
SMOOTHING CAPACITORS	ECO-S1KP822EA	8200uF 80V
2ND ORDER INPUT FILTER		
INPUT FILTER INDUCTOR	IHLP3232DZER1R0M11	1.0uH 18.2A $P_{loss} \cong 0.3W$
INPUT FILTER CAPACITOR	C5750X7S2A106M230KB	10uF CERAMIC 100V
INPUT FILTER DAMPING Rd	5-1625890-3	0.5Ω 1W Axial Resistor
INPUT FILTER DAMPING CAP	ECO-S1KA102CA	1000uF 80V
CONICAL SWITCHING CELL		
SWITCHING FREQ		600 KHZ
MOSFET	IRL520NPBF	100V 10A $P_{loss} \cong 37.7W$
SWITCHING DIODE	V12P10	100V 12A $P_{loss} \cong 2.9W$
2ND ORDER OUTPUT FILTER		
OUTPUT FILTER INDUCTOR	IHLP6767GZER15R0M11	15uH 14A $P_{loss} \cong 3.1W$
OUTPUT FILTER CAPACITOR	EEE-FC1H101P	100uF ELECTROLYTIC 50V
OUTPUT FILTER CAPACITOR	C5750X7S2A106M230KB	10uF CERAMIC 100V
CURRENT CHECK DIODE	V12P10	100V 12A
SENSE RESISTOR	MP915-0.10-1%	0.1Ω 15W (TO-126)
BJT-ZENER VOLTAGE SUPPLY		
VOLTAGE REGULATING BJT	TIP31C	100V 3A 2W
ZENER DIODE	1N4745ATR	16V 1W
CURRENT LIMITING RESISTOR	FMP200JR-52-2K7	2.7kΩ 2W
DRIVER VOLTAGE CAP	ECQ-V1H824JL	0.82uF FILM 50VDC
DRIVER VOLTAGE CAP	EKY-250ELL221MHB5D	220uF ELECTROYTIC 25V

COMPONENT / SPEC	MANUFACTURER PART #	ADDITIONAL SPECIFICATION
MOSFET DRIVER CIRCUIT		
MOSFET DRIVER	IR2125PBF	500VDC 1A
CURRENT PUMP DIODE	MUR120-TP	200V 1A
DRIVER ERROR CAPACITOR	ECQ-V1H153JL	0.015uF FILM 50VDC
CURRENT PUMP CAPACITOR	ECQ-V1H824JL	0.82uF FILM 50VDC
DRIVER OUTPUT RESISTOR		10Ω ¼ W
PWM PID CONTROLLER		
IC CONTROLLER	CYPRESS PSOC5® LP DEV KIT	